FILE NO. SM-CTV-O-081

COLOR TELEVISION

SERVICE MANUAL

MODELNO. 21E88
CHASSIS NO. CN-18EA

Please read this manual carefully before service.

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SPECIFICATIONS

Model Number		**21E88**
RF system	Color system	PAL, NTSC3.58, NTSC4.43
	Sound system	B/G, M, D/K, I
Video system		PAL4.43, NTSC3.58, NTSC4.43 (50/60Hz)
Programs preset		236 (0-235)
Antenna input		75Ω(unbalanced)
Picture tube Effective screen dimensions (Approx.)		406×305mm
Audio output (THD≤7%)		Main channel: 3W+3W
Power source		220V ~, 50Hz
Weight (Approx.)		23 Kg
Dimensions (W×H×D) (Approx.)		585×457×484mm
Rated power consumption		87W

Designs and specifications are subject to change without notice.

SAFETY INSTRUCTIONS AND MAINTENANCE

WARNING: BEFORE SERVICING THIS CHASSIS, READ THE "X-RAY RADIATION PRECAUTION", "SAFETY PRECAUTION" AND "PRODUCT SAFETY NOTICE" INSTRUCTION BELOW.

X-RAY RADIATION PRECAUTION

1. The EHT must be checked every time the TV is serviced to ensure that the CRT does not emit X-ray radiation as result of excessive EHT voltage. The maximum EHT voltage permissible in any operating circumstances must not exceed the rated value. When checking the EHT, use the High Voltage Check procedure in this manual using an accurate EHT voltmeter.
2. The only source of X-RAY radiation in this TV is the CRT. The TV minimizes X-RAY radiation, which ensures safety during normal operation. To prevent X-ray radiation, the replacement CRT must be identical to the original fitted as specified in the parts list.
3. Some components used in this TV have safety related characteristics preventing the CRT from emitting X-ray radiation. For continued safety, replacement component should be made after referring the PRODUCT SAFETY NOTICE below.
4. Service and adjustment of the TV may result in changes in the nominal EHT voltage of the CRT anode. So ensure that the maximum EHT voltage does not exceed the rated value after service and adjustment.

SAFETY PRECAUTION

WARNING: REFER SERVICING TO QUALIFIED SERVICE PERSONNEL ONLY.

1. The TV has a nominal working EHT voltage. Extreme caution should be exercised when working on the TV with the back removed.

1.1 Do not attempt to service this TV if you are not conversant with the precautions and procedures for working on high voltage equipment.

1.2 When handling or working on the CRT, always discharge the anode to the TV chassis before removing the anode cap in case of electric shock.

1.3 The CRT, if broken, will violently expel glass fragments. Use shatterproof goggles and take extreme care while handling.

1.4 Do not hold the CRT by the neck as this is a very dangerous practice.

2. It is essential that to maintain the safety of the customer all power cord forms be replaced exactly as supplied from factory.
3. Voltage exists between the hot and cold ground when the TV is in operation. Install a suitable isolating transformer of beyond rated overall power when servicing or connecting any test equipment for the sake of safety.

4. When replacing ICs, use specific tools or a static-proof electric iron with small power (below 35W).
5. Do not use a magnetized screwdriver when tightening or loosing the deflection yoke assembly to avoid electronic gun magnetized and decrement in convergence of the CRT.
6. When remounting the TV chassis, ensure that all guard devices, such as nonmetal control buttons, switch, insulating sleeve, shielding cover, isolating resistors and capacitors, are installed on the original place.
7. Replace blown fuses within the TV with the fuse specified in the parts list.
8. When replacing wires or components to terminals or tags, wind the leads around the terminal before soldering. When replacing safety components identified by the international hazard symbols on the circuit diagram and parts list, it must be the company-approved type and must be mounted as the original.
9. Keep wires away from high temperature components.

PRODUCT SAFETY NOTICE

CAUTION: FOR YOUR PROTECTION, THE FOLLOWING PRODUCT SAFETY NOTICE SHOULD BE READ CAREFULLY BEFORE OPERATING AND SERVICING THIS TV SET.

1. Many electrical and mechanical components in this chassis have special safety-related characteristics. These characteristics are often passed unnoticed by a visual inspection and the X-ray radiation protection afforded by them cannot necessarily be obtained by using replacements rated at higher voltages or wattage, etc. Components which have these special safety characteristics in this manual and its supplements are identified by the international hazard symbols on the circuit diagram and parts list. Before replacing any of these components read the parts list in this manual carefully. Substitute replacement components which do not have the same safety characteristics as specified in the parts list may create X-ray radiation.
2. Do not slap or beat the cabinet or CRT, since this may result in fire or explosion.
3. Never allow the TV sharing a plug or socket with other large-power equipment. Doing so may result in too large load, causing fire.
4. Do not allow anything to rest on or roll over the power cord. Protect the power cord from being walked on, modified, cut or pinched, particularly at plugs.
5. Do not place any objects, especially heavy objects and lightings, on top of the TV set. Do not install the TV near any heat sources such as radiators, heat registers, stove, or other apparatus that produce heat.
6. Service personnel should observe the SAFETY INSTRUCTIONS in this manual during use and servicing of this TV set. Otherwise, the resulted damage is not protected by the manufacturer.

SAFETY SYMBOL DESCRIPTION

The lightning symbol in the triangle tells you that the voltage inside this product may be strong enough to cause an electric shock. Extreme caution should be exercised when working on the TV with the back removed.

This is an international hazard symbol, telling you that the components identified by the symbol have special safety-related characteristics.

FDA This symbol tells you that the critical components identified by the FDA marking have special safety-related characteristics.

UL This symbol tells you that the critical components identified by the UL marking have special safety-related characteristics.

C UL This symbol tells you that the critical components identified by the C-UL marking have been evaluated to the UL and C-UL standards and have special safety-related characteristics.

VDE This symbol tells you that the critical components identified by the VDE marking have special safety-related characteristics.

MAINTENANCE

1. Place the TV set on a stable stand or base that is of adequate size and strength to prevent it from being accidentally tipped over, pushed off, or pulled off. Do not place the set near or over a radiator or heat register, or where it is exposed to direct sunlight.
2. Do not install the TV set in a place exposed to rain, water, excessive dust, mechanical vibrations or impacts.
3. Allow enough space (at least 10cm) between the TV and wall or enclosures for proper ventilation.
4. Slots and openings in the cabinet should never be blocked by clothes or other objects.
5. Please power off the TV set and disconnect it from the wall immediately if any abnormal condition are met, such as bad smell, belching smoke, sparkling, abnormal sound, no picture/sound/raster. Hold the plug firmly when disconnecting the power cord.
6. Unplug the TV set from the wall outlet before cleaning or polishing it. Use a dry soft cloth for cleaning the exterior of the TV set or CRT screen. Do not use liquid cleaners or aerosol cleaners.

ADJUSTMENTS

SET-UP ADJUSTMENTS

The following adjustments should be made when a complete realignment is required or a new picture tube is installed.

Perform the adjustments in the following order:

1. Color purity
2. Convergence
3. White balance

Notes:

① The purity/convergence magnet assembly and rubber wedges need mechanical positioning.

② For some picture tubes, purity/ convergence adjustments are not required.

1. Color Purity Adjustment

Preparation:

Before starting this adjustment, adjust the vertical sync, horizontal sync, vertical amplitude and focus.

1.1 Face the TV set north or south.

1.2 Connect the power plug into the wall outlet and turn on the main power switch of the TV set.

1.3 Operate the TV for at least 15 minutes.

1.4 Degauss the TV set using a specific degaussing coil.

1.5 Set the brightness and contrast to maximum.

1.6 Counter clockwise rotate the R /B low brightness potentiometers to the end and rotate the green low brightness potentiometer to center.

1.7 Receive green raster pattern signals.

1.8 Loosen the clamp screw holding the deflection yoke assembly and slide it forward or backward to display a vertical green zone on the screen. Rotate and spread the tabs of the purity magnet around the neck of the CRT until the green zone is located vertically at the center of the screen.

1.9 Slowly move the deflection yoke assembly forward or backward until a uniform green screen is obtained.

1.10 Tighten the clamp screw of the assembly temporarily. Check purity of the red raster and blue raster until purities of the three rasters meet the requirement.

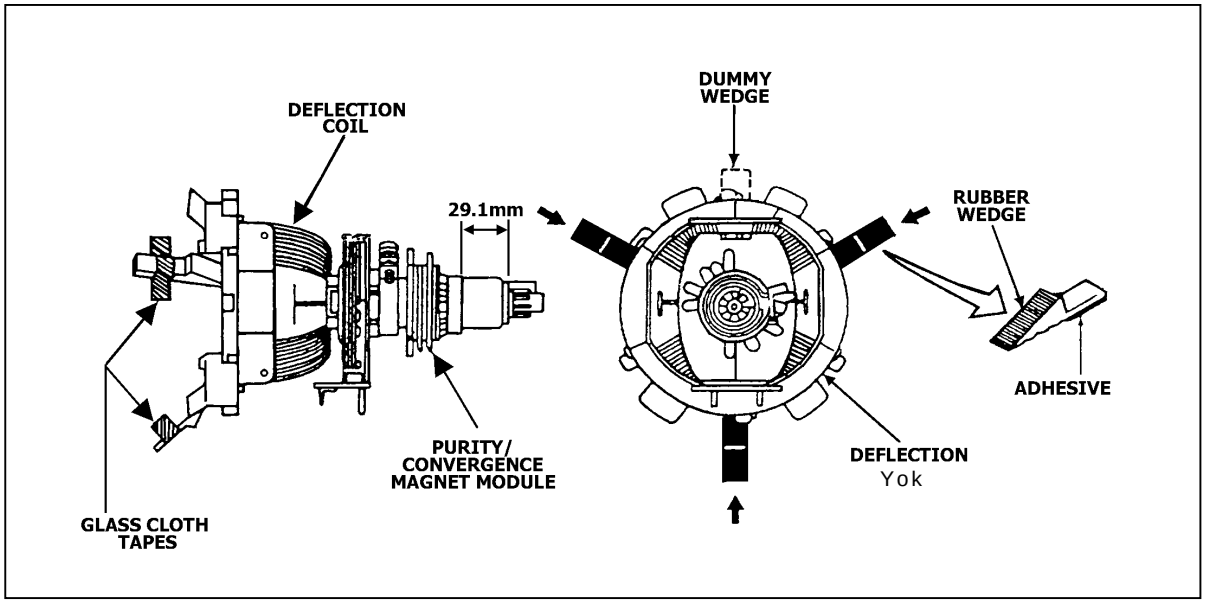


Fig. 1

2. Convergence Adjustment

Preparation:

Before attempting any convergence adjustment, the TV should be operated for at least 15 minutes.

2.1 Center convergence adjustment

2.1.1 Receive dot pattern.

2.1.2 Adjust the brightness/contrast controls to obtain a sharp picture.

2.1.3 Adjust two tabs of the 4-pole magnet to change the angle between them and red and blue vertical lines are superimposed each other on the center of the screen.

2.1.4 Turn both tabs at the same time keeping the angle constant to superimpose red and blue horizontal on the center of the screen.

2.1.5 Adjust two tabs of the 6-pole magnet to superimpose red/blue line and green line.

2.1.6 Remember red and blue movement. Repeat steps 2.1.3～2.1.5 until optimal convergence is obtained.

2.2 Circumference convergence adjustment

2.2.1 Loosen the clamp screw holding the deflection yoke assembly and allow it tilting.

2.2.2 Temporarily put the first wedge between the picture tube and deflection yoke assembly. Move front of the deflection yoke up or down to obtain better convergence in circumference. Push the mounted wedge in to fix the yoke temporarily.

2.2.3 Put the second wedge into bottom.

2.2.4 Move front of the deflection yoke to the left or right to obtain better convergence in circumference.

2.2.5 Fix the deflection yoke position and put the third wedge in either upper space. Fasten the

deflection yoke assembly on the picture tube.

2.2.6 Detach the temporarily mounted wedge and put it in either upper space. Fasten the deflection yoke assembly on the picture tube.

2.2.7 After fastening the three wedges, recheck overall convergence and ensure to get optimal convergence. Tighten the lamp screw holding the deflection yoke assembly.

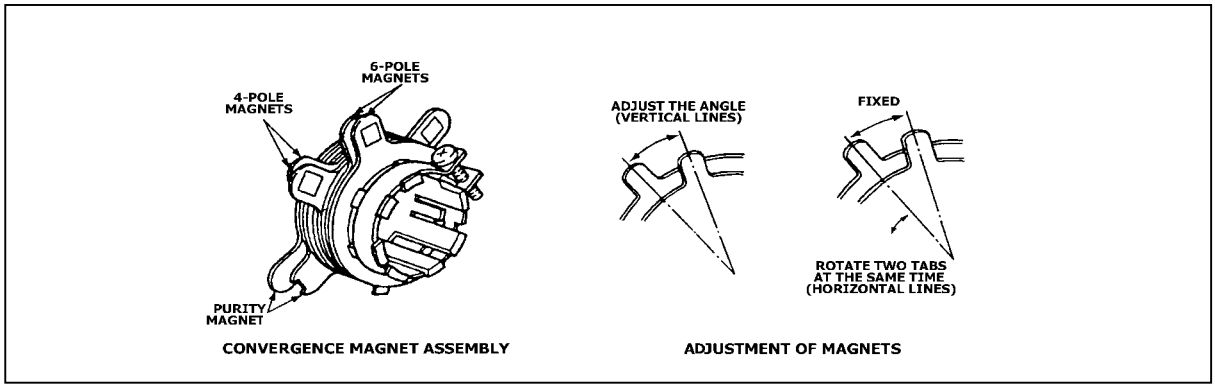


Fig. 2

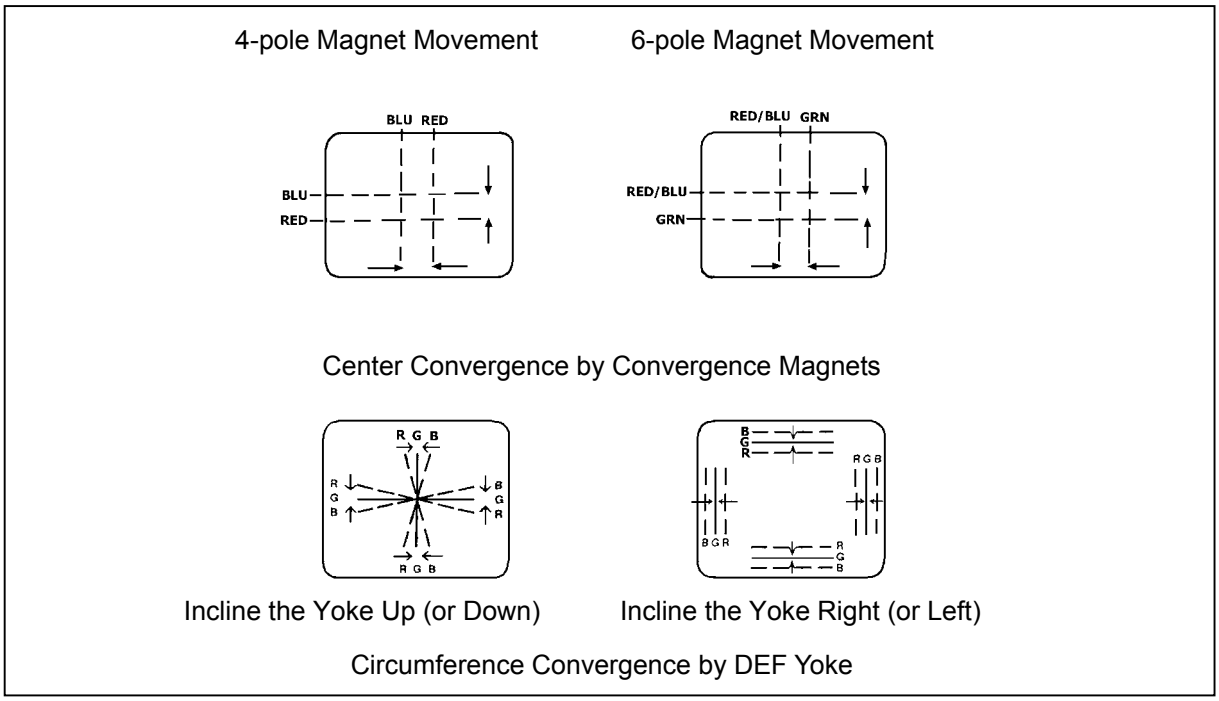


Fig.3

3. White Balance Adjustment

Generally, white balance adjustment is made with professional equipment. It's not practical to get good white balance only through manual adjustment. For TVs with I^2C bus control, change the bus data to adjust white balance.

CIRCUIT ADJUSTMENTS

Preparation:

Circuit adjustments should be made only after completion of set-up adjustments.

Circuit adjustments can be performed using the adjustable components inside the TV set. For TVs with I^2C bus control, first change the bus data.

1. Degaussing

A degaussing coil is built inside the TV set. Each time the TV is powered on, the degaussing coil will automatically degauss the TV. If the TV is magnetized by external strong magnetic field, causing color spot on the screen, use a specific degausser to demagnetize the TV in the following ways. Otherwise, color distortion will be shown on the screen.

1.1 Power on the TV set and operate it for at least 15 minutes.

1.2 Receive red full-field pattern.

1.3 Power on the specific degausser and face it to the TV screen.

1.4 Turn on the degausser. Slowly move it around the screen and slowly take it away from the TV.

1.5 Repeat the above steps until the TV is degaussed completely.

2. Confirmation and Adjustment for Voltage

Caution: +B voltage has close relation to high voltage. To prevent X-ray radiation, set +B voltage to the rated value.

2.1 Make sure that the supply voltage is within the range of the rated value.

2.2 Connect a digital voltmeter to the voltage output terminal of the main PCB. Power on the TV and set the brightness and sub-brightness to minimum. Ensure that the voltage from the main PCB reads as follows.

2.3 Regulate voltage adjustment components on the power section until the +B the voltage reaches the rated value.

Table 1

Test Point	Voltage (V)
Negative of VD851	118V±2V
Negative of VD852	17V±1V
Negative of VD854	11V±1V
Negative of VD857	$14V\ ^{+1V}_{-1.5V}$
Positive of C874	9V±0.5V
Positive of C878	5V±0.5V
Positive of C800	5V±0.25V

Note:

It's impossible to check the power part separately from the main chassis board as the part is mounted on the main chassis board. The power components, etc. should be checked for burnout when power-on. If burned out, do not power on the TV again until the cause is found out.

3. High Voltage Inspection

Measure voltages of test points on the main PCB with the digital voltmeter. Measure the CRT high voltage with the high-voltage testing equipment and heater voltage with the high-frequency effective voltmeter. The rated values are shown as below.

Table 2

Test Point	Voltage (V)
Negative of VD603	25±1.5V (for BSC6OU FBT only) 27±1.5V (for BSC62V1 FBT only)
Negative of VD855A	195±5.0V
CRT anode	25±1.5KV (for IRICO，SHANGHAI NOVEL, LG, CHUNGHWA，and THAI CRTs) 27±1.5KV (SAMSUANG，BMCC)
Heater	6.3±0.3Vrms

4. Focus Adjustment

Caution: Dangerously high voltages are present inside the TV. Extreme caution should be exercised when working on the TV with the back removed.

4.1 After removing the back cover, look for the FBT on the main PCB. There should be a FCB on the FBT.

4.2 Power on the TV and preheat it for 15 min.

4.3 Receive a normal TV signal. Rotate knob of the FCB until you get a sharp picture.

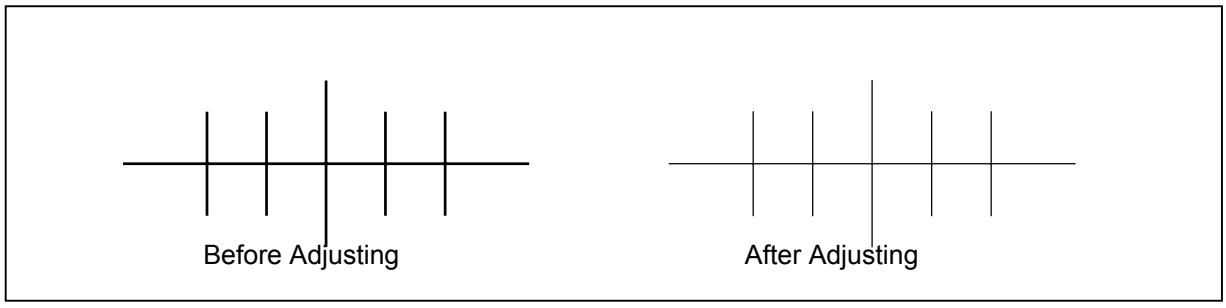


Fig. 4

5. Safety Inspection

5.1 Inspection for insulation and voltage-resistant

Perform safety test for all naked metal of the TV. Supply high voltage of 3000V AC, 50Hz (limit current of 10mA) between all naked metal and cold ground. Test every point for 3 sec. and ensure no arcing and sparking.

5.2 Requirements for insulation resistance

Measure resistance between naked metal of the TV and feed end of the power cord to be infinity with a DC-500 high resistance meter and insulation resistance between the naked metal and degaussing coil to be over 20MΩ.

6. SERVICE mode

6.1 To enter the DESIGN/SERVICE mode

Set the volume to 0. Then press and hold the MUTE button on the remote control, and press the MENU button on the TV to enter the SERVICE mode. In this case, red "S" is displayed on the upper center of the screen. To exit from the S mode, turn off the TV set by the POWER button on the remote control.

Caution: The user service mode adjustment can be changed only when service personnel adjust the whole set data during servicing. As the control data have dramatic effects on functions and performance of the TV, service personnel should not tell user how to enter the SERVICE mode to avoid improper data settings.

6.2 Adjustments and bus data (CH08T0603)

Table 3 Function Description for Bus Data

	Bit	Function Description	Status
MODE0	Bit7.6	Audio system options (available during auto search and use of AUTO button)	00: B/G 01: I 10: D/K 11: M
	Bit5	SECAM INHIBIT	00: SECAM gate pulse width, 2.2 usec 01: 2.0 usec 10: 1.8 usec 11: SECAM demodulation inhibit
	Bit4		
	Bit3	V MUTE	When changing channels: 0: Y-MUTE 1: RGB MUTE
	Bit2	SECAM	0: No 1: Yes
	Bit1	AUTO2	0: PAL 1: Without PAL
	Bit0	Power-on modes	0: Memory on 1: Soft on

(continued)

MODE1	Bit7	Write-in LOGO	0: No 1: Yes
	Bit6	NICAM DK for CHINA	0: No 1: Yes
	Bit5	With two sets of AV terminals, refresh AV terminals ?	0：Yes (Recommended) 1：No
	Bit4	Screen saver	0: No 1: Yes
	Bit3	M	0: No 1: Yes
	Bit2	D/K	0: No 1: Yes
	Bit1	I	0: No 1: Yes
	Bit0	B/G	0: No 1: Yes
MODE2	Bit7	NO USE	
	Bit6	Small character processing program	0: New program (Recommended) 1: Old program
	Bit5	RF NTSC options	0: No 1: Yes
	Bit4	Power-on message display	1: Yes 0: No (Recommended)
	Bit 3	NICAM sound with MDB	0: No 1: Yes
	Bit 2	Mono system	1: Yes 0：No
	Bit 1	Single language	1: Yes 0：No
	Bit.0	TA1343 woofer or MDB output mode options	0: Mono output 1: Overlapped to main channel（Recommended）
MODE3	BIT 7	Childlock vertical bug processing	0: Yes (Recommended) 1:No
	BIT 6	Horizontal AFC bug processing	0: Yes (Recommended) 1:No
	BIT 5	DVD option	1: No 0: Yes (Recommended)
	BIT.4	Step length setting for lighting up gradually during power-on	1: Large step (Recommended) 0：Small step

(continued)

	BIT 3	Option bit for default language by AUTO button and initialization	0: Chinese 1: English
	BIT 2	PWM output option	0: No 1: Yes
	BIT 1	Instant on	1: Yes 0：No
	BIT 0	AV Switch 4053 option	0: No 1: Yes
MODE4	BIT 7	Audio processing IC (SOUND menu)	0: No 1: Yes
	BIT 6	Woofer option in SOUND menu	0: No 1: Yes
	BIT 5	TA1343 option	0: No 1: Yes
	BIT 4	MSP3410G option (NICAM)	0: No 1: Yes
	BIT 3	NJW1161 option (SRS IC)	0: No 1: Yes
	BIT 2	NJW1160 option (BBE IC & SRS IC)	0: No 1: Yes
	BIT 1	NJW1137 option (BBE IC)	0: No 1: Yes
	BIT 0	Soft IIC option	0: No 1: Yes
OPT	Bit 7	No use	
	Bit 6	VCO adjustments	0: PIF VCO functions (PIFVCO = 10) during auto search and search； 1: PIFVCO = 10 during turn-on，and PIFVCO = 00 in Normal mode
	Bit 5	No use	
	Bit 4	Large-amplitude AFT switch when no signal	1: Off 0: On
	Bit 3	Audio gain switch	0：927mVrms at 25kHz/dev 1：500mVrms at 25kHz/dev

(continued)

	Bit 2	Y-MUTE	0: No 1: Yes
	Bit 1	No use	
	Bit 0	No use	
OSD	Horizontal position of OSD		
RCUT	R cut off		
GCUT	G cut off		
BCUT	B cut off		
GDRV	G drive		
BDRV	B drive		
CNTX	Contrast Max.		
BRTC	Bright center		
COLC	Color center (for NTSC)		
TNTC	Tint center (for NTSC)		
TNTCAV	Tint center in VIDEO mode(for NTSC)		
COLP	Color center (for PAL)		
COLS	Color center (for SECAM)		
DCOL	DVD color		
SCOL	Sub color center (for DVD)		
SCNT	Y-sub contrast		
CNTC	Contrast center		
CNTN	Contrast Min.		
BRTX	Bright Max.		
BRTN	Bright Min.		
COLX	Color Max.		

(continued)

COLN	Color Min.		
TNTX	Tint Max.		
TNTN	Tint Min.		
ST3	Sharp center for NTSC 3.58 (TV)		
SV3	Sharp center for NTSC 3.58 (VIDEO)		
ST4	Sharp center for other color system (TV)		
SV4	Sharp center for other color system (VIDEO)		
SVD	Sub sharp center in DVD		
ASSH	Asymmetry sharpness		
SHPX	Sharpness Max.		
SHPN	Sharpness Min.		
TXCX	Text RGB in user contrast Max.		
RGCN	Text RGB in user contrast Min.		
ABL	Bit 5	Y peak limiter	0: Off 1: On
	Bit 4	OSD ABL	0: Active 1: Inactive
	Bit 3.2	ABL start point	00: ABL start point: 0V 01: -0.15V 10: -0.30V 11: -0.45V
	Bit 1.0	ABL gain	00: -0.2V 01: -0.4V 10: -0.6V 11: -0.8V
DCBS	Bit 7	Blank SW	0: H, V blanking on 1: H, V blanking off
	Bit 6		
	Bit 5.4	OSD level	00: OSD level, 80 IRE 01: 70IRE 10: 60IRE 11: 50IRE
	Bit 3.2	Y gamma	00: Off 01: Y point 90 IRE, Gain –3dB 10: 80IRE 11: 70IRE

(continued)

	Bit 1.0	Black stretch	00: Off 01: Black stretch point, 25 IRE 10: 35IRE 11: 45IRE
CLTO Chroma data (TV&not M) CLTM (TV&M) CLVD (DVD) CLVO (50hz) /CLVM （60hz） (VIDEO)	Bit 7	Killer off	0: Normal 1: Always killer off
	Bit 6	P/N ID	0: PAL/ NTSC killer sensitivity, 1mVpp 1: 10mVpp
	Bit 5	C gamma	0: Color gamma off 1: On
	Bit 4.3	NTSC matrix	00: USA (105 degree) 01: Japan (93 degree) 10: DVD 11:
	Bit 2.1.0	Y DL	000: -40 nsec 001: 0 010: 40 nsec 011: 80 nsec 100: 120 nsec 101: 160 nsec 110: 200 nsec 111: 240 nsec
DEF	BIT0 = 0: V AGC reference depends on YC VCC; BIT0 = 1: V AGC reference depends on integrated regulator		
SECD	No use		
HPOS	50hz horizontal phase		00: -3usec 10: 01F: +3usec
VP50	V phase (50Hz)		0: V phase delay, 0H 7: 7H
HIT	V size		00: -50% 20: 0% 3F: 50%
HPS	Adjusting difference between horizontal centers in PAL and NTSC		
VP60	V phase (60Hz)		0: V phase delay, 0H 7: 7H
HITS	Adjusting difference between vertical amplitudes in PAL and NTSC		
VLIN	V-linearity		0: -15% 8: 0% F: 15%
VSC	V-S correction		0: -16% 8: 0% F: 16%

(continued)

VLIS	Adjusting difference between vertical linear in PAL and NTSC	
VSS	Shift data of 50 Hz/ 60 Hz Correction	
DPC	No use	
DPCS	No use	
HIT69	Vertical amplitude in 16:9 mode (PAL)	
DPC69	No use	
HIT69S	Vertical amplitude in 16:9 mode (NTSC)	
DPC69S	No use	
KEY	No use	
KEYS	No use	
WID	No use	
WIDS	No use	
ECCT	No use	
ECCB	No use	
VEHT	No use	
HEHT	No use	
SBY	Use in SECAM	
SRY	Use in SECAM	
BRTS	Sub bright (difference)	
RFAGC	RF AGC	00: IF mute 01: 65dBu 3F: 100dBu

(continued)

HAFC	BIT 3.2	AFC gain (in VIDEO mode)	Data / Description Blanking Period / Picture Period 0 0 — 3 — 1 0 1 — 4/7 — 2/7 1 0 — 4/3 — 1 1 1 — Off — Off
	BIT 1.0	AFC gain (in TV mode)	Data / Description Blanking Period / Picture Period 0 0 — 3 — 1 0 1 — 4/7 — 2/7 1 0 — 4/3 — 1 1 1 — Off — Off
V01	Volume output data at 1%		
V25	Volume output data at 25%		
V50	Volume output data at 50%		
V100	Volume output data at 100%		
Woofer	TA1343 woofer Max.		
STAT	No use		
FLG0	Bit 7	VCO readjust when position select	0: Enable 1: Disable
	Bit 2	N buzz cancel	0: Nyquist buzz cancel, on 1: Off
	Bit 1	AFT window SW	0: Wide (-/+ 250kHz) AFT sensitivity, for channel search 1: Narrow (-/+ 83kHz) for normal operation
	Bit 0	Over modulation	0: Normal 1: PIF over modulation switch on
FLG1	Bit 5	MIX gain	0: SIF 1MHz convert gain, low gain 1: High gain
	Bit 4	Sync separation.	0: Sync separation level 40% 1: 36%
REFP	AKB pulse position		000: 0H 001: 1H 010: 2H 011: 3H 100: 4H 101: 5H 110: 6H 111: 7H

(continued)

RSNS	R sense		00: x 0 20: x 0.5 3F: x 1.0
GSNS	G sense		00: x 0 20: x 0.5 3F: x 1.0
BSNS	B sense		00: x 0 20: x 0.5 3F: x 1.0
MOD	Bit 6.5.4	PIF frequency	001: 45.75 MHz 011: 38.9 MHz 100: 38.0 MHz
	Bit 1.0	AKB mode	00: AKB off 01: ACB (cutoff: align to targets) 10: ADB (drive: align to targets) 11: AKB (cutoff/drive: align to targets)
STBY	Bit 3.2	VCD standby	00: Normal 01: Normal 10: Normal 11: VCD standby
	Bit 1.0	IF standby	00: Normal 01: Normal 10: Normal 11: IF standby
SVM	No use		
SVM1	No use		
SVM3	No use		
VBLK	BIT 3.2	V blanking stop point	00: 310H(50hz) 263H(60hz) 01: 299H(50hz) 254H(60hz) 10: 295H(50hz) 250H(60hz) 11: 291H(50hz) 246H(60hz)
	BIT 1.0	V blanking start point	00: 23H(50hz) 22H(60hz) 01: 33H (50hz)30H(60hz) 10: 37H (50hz)34H(60hz) 11: 41H(50hz) 38H(60hz)
VCEN	Vertical centering		00: -32% 20: 0% 3F: 30%
UCOM	Bit 1.0	Internal ADC	00: GND 01: R output 10: B output 11: Monitor RF AGC via ADC
	Bit 5.4.3	Improving NTSC color signal-to-noise ratio	Available range: 000....011

(continued)

VTST	No use	
PYNX	Normal H.SYNC Max.	0----------3F
PYNN	Normal H.SYNC Min.	0----------3F
PYXS	ASM/search H.SYNC Max.	0----------3F
PYNS	ASM/search H.SYNC Min.	0----------3F
BASC	Bass volume center	
BASX	Bass volume Max.	
TREC	Treble volume center	
BALC	Balance volume center	
BAS1	BASS IN MUSIC MODE SET	
TRE1	Treble in MUSIC mode set	
WFL1	Woofer in MUSIC mode set	
BAS2	Bass in NEWS mode set	
TRE2	Treble in NEWS mode set	
WFL2	Woofer in NEWS mode set	
BAS3	Bass in THEATRE mode set	
TRE3	Treble in THEATRE mode set	
WFL3	Woofer in THEATRE mode set	
WON1	TA1343 Max. woofer setting. The bigger the setting the smaller Max. woofer	
WON2	Woofer liner set	
FVOL	Prescale FM/AM (No use in simple version)	
NVOL	Prescale NICAM (No use in simple version)	
EVOL	Prescale SCART input (No use in simple version)	
NICL	NICAM->MONO level (No use in simple version)	

(continued)

NICH	MONO->NICAM level (No use in simple version)		
NOIS	Bit 2	AFC gain data setting in TV mode: 1: Adjust HAFC gain in the lowest two bits of HAFC 0: With weak signal received, AFC gain = 0x10; with strong signal received, AFC gain = 0x00	
	Bit 7- Bit 0	Criterion of signal strength: >NOIS: Weak signal <= NOIS: Strong signal	
VATT	Audio ATT 00:-85DB or less 7F:0DB (7 BITS)		
COM1	No use		
COM2	No use		
EQU1(12345)	NICAM chip five-equalizer data when the sound mode set to MUSIC: (No use in simple version) B11 (for 120Hz) B12 (for 500 Hz) B13 (for 1.5KHz) B14 (for 5KHz) B15 (for 10KHz)		
EUQ2(12345)	NICAM chip five-equalizer data when the sound mode set to NEWS: (No use in simple version) B21 (for 120Hz) B22 (for 500 Hz) B23 (for 1.5KHz) B24 (for 5KHz) B25 (for 10KHz)		
EQU3(12345)	NICAM chip five-equalizer data when the sound mode set to THEATRE: (No use in simple version) B31(for 120Hz) B32 (for 500 Hz) B33 (for 1.5KHz) B34 (for 5KHz) B35 (for 10KHz)		
BBE	Highest four bits :BBE Low contour(0dB to 15dB) ;Lowest four bits: BBE process(0dB to 15dB)		
OSDF	OSD frequency set		
LANG	Bit 1	Chinese	1: Yes 0: No
	Bit 0	English	1: Yes 0: No
MDB68 (0x49)	MDB effect strength		00 hex MDB OFF (default) (No use in simple version) 7F hex maximum MDB
MDB6A (0x30)	MDB harmonic content		(No use in simple version) 00 hex no harmonics are added (default) 64 hex 50% fundamentals + 50% harmonics 7F hex 100% harmonics

(continued)

MDB6C (0x07)	MDB high pass corner frequency	(No use in simple version) 2 20 Hz 3 30Hz 30 300 Hz
MDB6B (0x08)	MDB low pass corner frequency	(No use in simple version) 5 50 Hz 6 60Hz 30 300 Hz
Mdb2dh (0x14)	Subwoofer corner frequency	(No use in simple version) corner frequency in 10 Hz steps (range: 50...400 Hz)
Mdb2dL (0x02)	Subwoofer complementary high-pass filter	(No use in simple version) 00 hex loudspeaker channel unfiltered 01 hex a complementary high-pass is processed in the loud-speaker output channel 02 hex MDB is set to OVERLAP mode

Table 5 Bus Data

item	data	item	data	item	data	item	data
MODE0	3D	GDRV	40	CLTS	40	BSNS	00
MODE1	1F	BDRV	40	CLVO	65	MOD	40
MODE2	09	CNTX	7F	CLVD	60	STBY	00
MODE3	18	BRTC	40	DEF	01	SVM	00
MODE4	90	COLC	40	AKB	00	VBLK	00
LANG	03	TNTC	48	SECD	18	VCEN	16
BBE	9C	TNTCAV	48	HPOS	0C	UCOM	00
MDB68	40	COLP	F8	VP50	03	VTST	00
MDB6A	30	COLS	40	HIT	27	PYNX	2E
MDB6C	0A	DCOL	20	HPS	03	PYNN	18
MDB6B	0A	SCOL	00	VP60	00	PYXS	22
Mdb2dh	14	SCNT	0B	HITS	01	PYNS	1E
Mdb2dL	02	CNTC	40	VLIN	08	BASC	40

(continued)

EQU11	64	CNTN	01	VSC	04	BASX	70
EQU12	64	BRTX	25	VLIS	00	TREC	40
EQU13	64	BRTN	15	VSS	00	BALC	40
EQU14	64	COLX	3F	HIT69	14	BAS1	64
EQU15	64	COLN	00	HIT69S	01	BAS2	20
EQU21	4B	TNTX	28	SBY	05	BAS3	50
EQU22	19	TNTN	28	SRY	0C	TRE1	64
EQU23	4B	ST3	25	BRTS	00	TRE2	20
EQU24	19	SV3	30	RAGC	20	TRE3	50
EQU25	4B	ST4	25	HAFC	09	WFL1	64
EQU31	32	SV4	30	V01	37	WFL2	00
EQU32	4B	SVD	30	V25	60	WFL3	64
EQU33	32	ASSH	07	V50	6F	WON1	01
EQU34	4B	SHPX	3F	V100	7F	WON2	00
EQU35	32	SHPN	20	woofer	60	FVOL	0A
OSDF	64	TXCX	3F	STAT	00	NVOL	5F
OSD	20	RGCN	1F	FLG0	06	EVOL	18
OPT	60	ABL	37	FLG1	08	NICL	0A
RCUT	40	DCBS	13	REFP	00	NICH	17
GCUT	38	CLTO	66	RSNS	00	NOIS	01
BCUT	35	CLTM	63	GSNS	00	VATT	70

Notes:

① The data sheet may differ dependent on different models.

② The data sheet may differ dependent on different CRTs for the same model.

③ The data marked with “ * ” can be adjusted.

CONTROL BUTTONS

1. CONTROL BUTTONS

Front panel

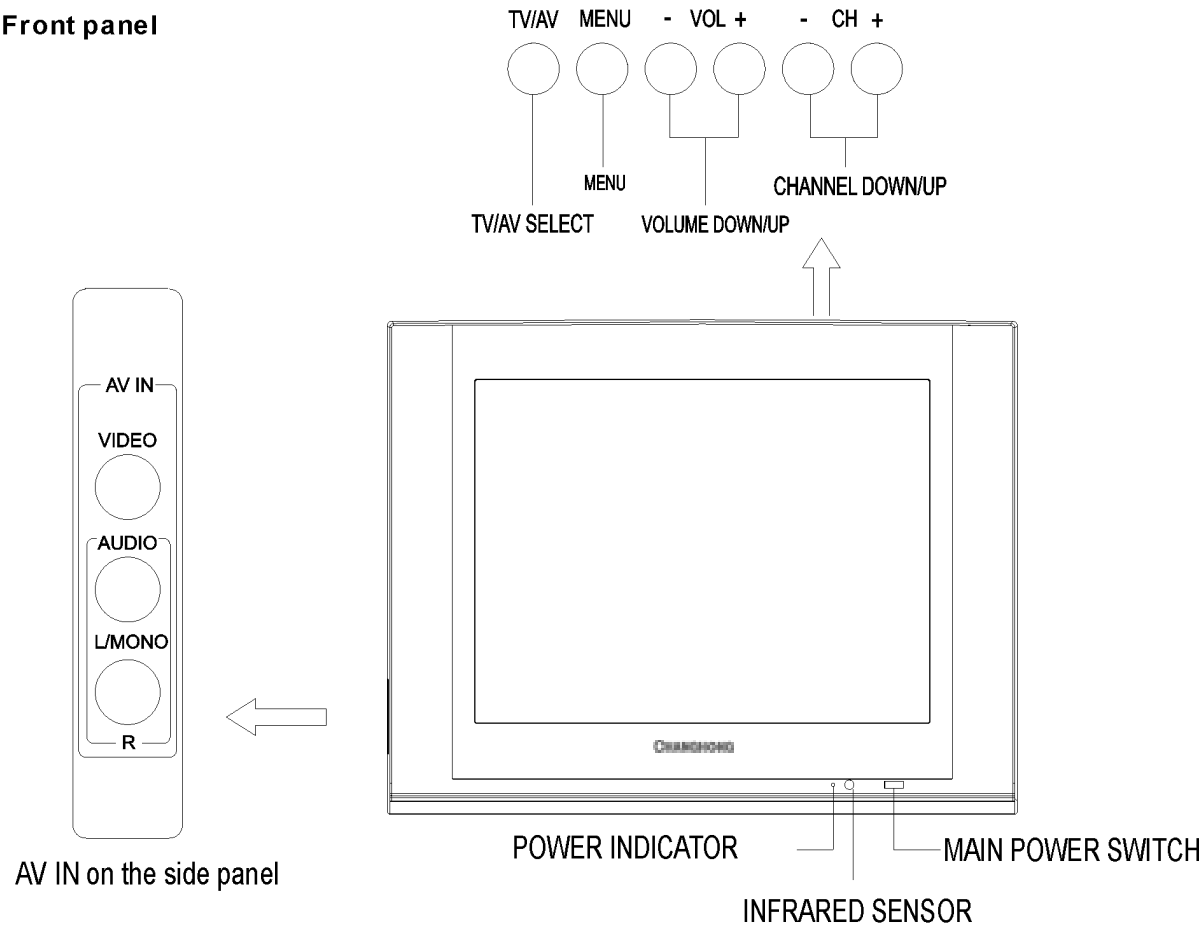


Fig. 5 Front panel

Rear panel

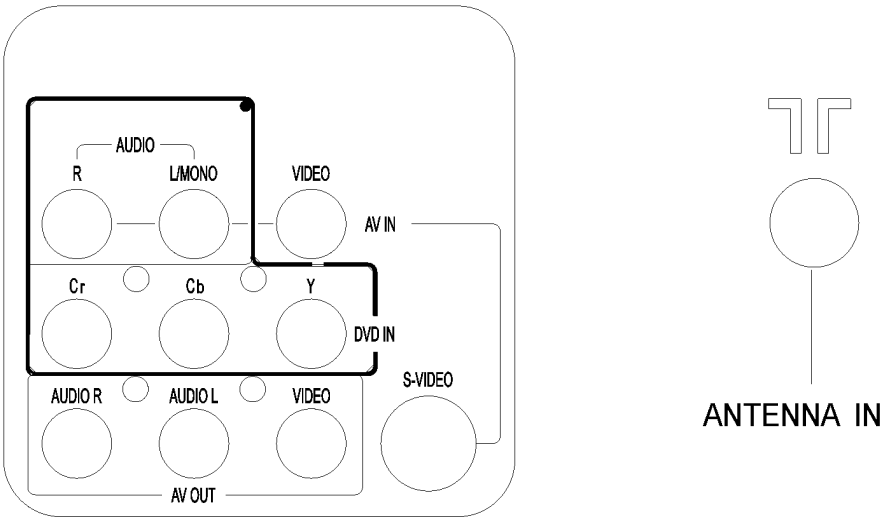


Fig. 6 Rear panel

2. REMOTE CONTROL

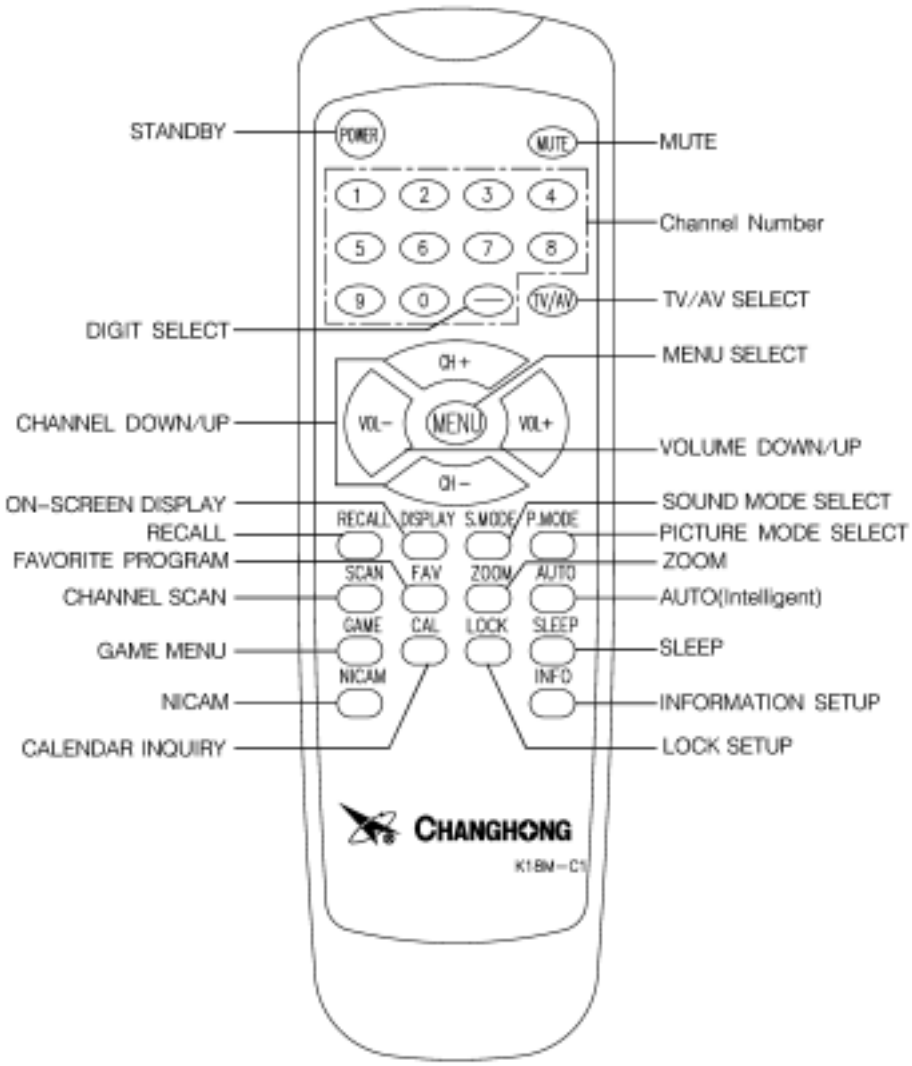


Fig. 7 Remote control

Notes:

(1) When in operation please point your remote control directly to the infrared sensor.

(2) Do not expose the remote control to impacts water or disassemble it.

(3) Do not repeatedly press the buttons on the remote control. Allow interval of no less than two seconds.

3. BASIC FUNCTIONS

Power On/Off

1. Memory power on

Plug in the supply socket and press the **MAIN POWER SWITCH** on the TV. The TV enters the former mode before Power-off i.e. the TV directly enters the TURN ON mode if in the TURN ON mode before power-off, or enters the STANDBY mode if in the STANDBY mode before power-off. In this case, you may press any of the **POWER**, **CH-/CH+**, **0-9** buttons on the remote control or **CH-/CH+** on the TV to turn on the TV.

2. Power off

When the TV in the TURN ON mode, press the **POWER** button to shift the TV to the STANDBY mode, press the **MAIN POWER SWITCH** directly to power off the TV at once.

Part of circuit on the TV remains active in the STANDBY mode. To cut off the power off completely, please press the **MAIN POWER SWITCH**.

Note:

Avoid switching the TV on and off frequently. Doing so may shorten life span of internal components.

General Operation

1. **Intelligent operation**

By this function, the TV can accomplish many important operation and settings, which is convenient for your operation.

1) Press the **AUTO** button and hold it for 2 sec so that the TV automatically completes some settings, such as settings for color/sound systems, picture/sound modes and volume.

2) After completion, the screen message “ASM?” is displayed. At this time, press the **AUTO** button again and the TV enters the ASM mode. It returns to CH No.1 after ASM. You may watch the TV program now.

· If with TUNING LOCK ON, the screen message “ASM?” will not appear and ASM doesn’t begin.

2. Channel selection

1) Pressing the **CH-/CH+** buttons can select another lower-numbered or upper-numbered channel.

2) Direct selection

*To select a one-digit channel number

Press the -- button to choose “ -” firstly, then press one of **0-9** buttons.

*To select a two-digit channel number

Press the -- button to choose “ - -” firstly, then enter a first-digit and second-digit.

*To select a three-digit channel number

Press the -- button to choose “ - - -” firstly, then enter a first-digit, second-digit and third-digit.

Note: Each digit should be entered at 3 sec. time interval.

3) Program scan

Press the **SCAN** button and the “SCAN OFF” appear on the screen. Press the button again and the TV begins to scan from the current channel. To stop scan and start the corresponding operation, press any other buttons. The channel skipped cannot appear on the screen during scan.

4) Recall

Press the **RECALL** button and the TV will directly skip back to the previous program.

3. On-screen display

Press the **DISPLAY** button repeatedly in the TV or AV mode to display the current information on the screen and turn off the display respectively.

With other OSD, pressing the **DISPLAY** button first can turn it off.

4. Volume control

1) Press the **VOL-/VOL+** buttons to decrease or increase the volume. Adjustable range, 0～100
2) During normal play, press the **MUTE** button and the sound is eliminated. The TV will display a red character on the screen.

To cancel MUTE, you may press the **MUTE** button again or the **VOL+** buttons.

5. NICAM

Press the **NICAM** button to switch the TV among the following mode depending on signals received. If without NICAM, the button doesn't function.

1) If with NICAM bilingual signals received press the **NICAM** button to switch the TV among the "△", " I " and " II " modes.
2) If with NICAM stereo signals received press the **NICAM** button to swith the TV among the "∞ " and "△" modes.

Menus

Many operations get start from menu selection.

When watching TV programs, press the **MENU** button to display menu. Use the **VOL-/VOL+** buttons repeatedly to highlight one of PICTURE, SETUP, TUNING TIMER and OPTION menus cyclically. Use the **CH+/CH-** buttons to access a menu (hand cursor is displayed before the highlighted item and the characters turn colored).

After calling up the menu, press the **CH+/CH-** buttons to select an adjustment, and press the **VOL-/VOL+** or **Channel Number** buttons to adjust as per the prompt on bottom of the screen.

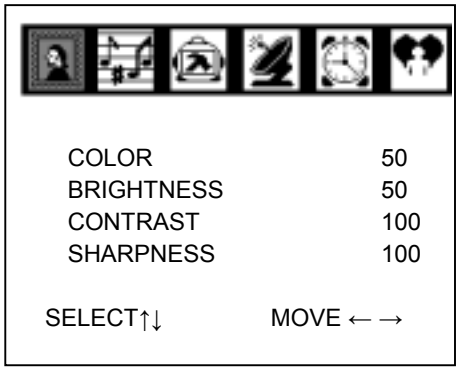


Fig. 8

Press the **LOCK, INFO** or **GAME** button to access the related menu and use the way mentioned above to adjust.

Menu selections are omitted in the following function presentation.

The buttons on the TV share the same functions with those buttons of the same name on the remote control. If your remote control becomes invalid or lost, you can use many basic functions by pressing the buttons on the TV.

Note: In the AV mode, TUNING menu is not available.

Tuning in

This section gives descriptions about adjustment of items in the **TUNING** menu.

1. Auto search

After selecting “ASM” in the TUNING menu, press the **VOL+** button. The TV will search automatically in sequence. After auto search, the TV will store receivable channels and returns to CH NO. 1. Unused channel number is automatically set to SKIP ON.

During auto search, press the VOL- button to stop searching.

Note:

During ASM, the Color system is generally set to AUTO and Sound system to BG.

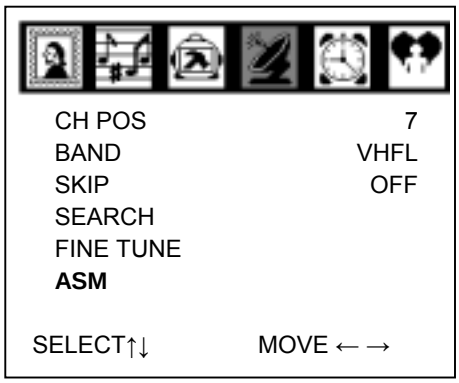


Fig. 9

2. Search

In case the desired channel cannot be preset with the ASM function, or you would like to set the desired channels to specific channel numbers, please use the SEARCH function.

After setting the desired BAND in the TUNING menu, select “SEARCH” and press the **VOL-/VOL+** buttons. The TV searches another lower/upper channel. To stop search, press the **MENU** button.

If the selected channel is not the one you want, press the **VOL-/VOL+** buttons again until the desired channel is selected. If the TV does not stop searching when finding a channel, please use the FINE TUNE function.

3. Frequency fine-tuning

After selecting “FINE TUNE” in the TUNING menu, press and hold down the **VOL-/VOL+** buttons until you get the best sound and picture effect.

4. Skip

After auto search, there may be some repeated program or inferior signals received. Skipping the undesired program position can dramatically quicken channel selection.

Select “SKIP” in the TUNING menu, then press the **VOL-/VOL+** buttons to set “SKIP ON”. After the TUNING menu disappears, press the **CH-/CH+** buttons and you will find the channel number skipped. If you select the channel number by the **Channel Number** buttons, the channel number has changed to red.

To resume the channel number that has been skipped, repeat the operations mentioned above. Then set “SKIP OFF”.

STRUCTURE AND CHASSIS FUNCTION

1. STRUCTURE BLOCK DIAGRAM

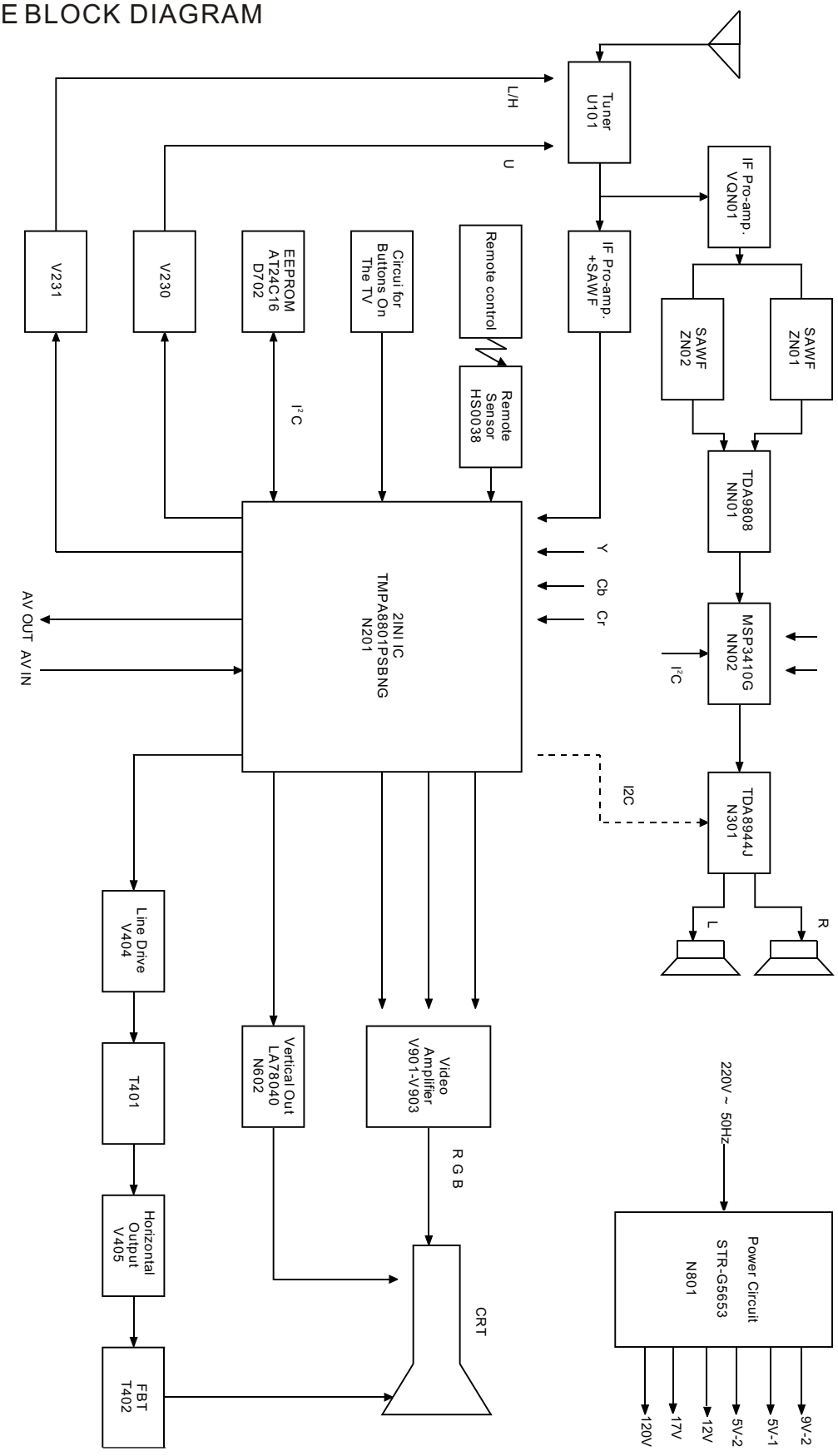


Fig. 10 Structure Block Diagram for CN-18EA Chassis

2. BLOCK DIAGRAM FOR SUPPLY VOLTAGE SYSTEM

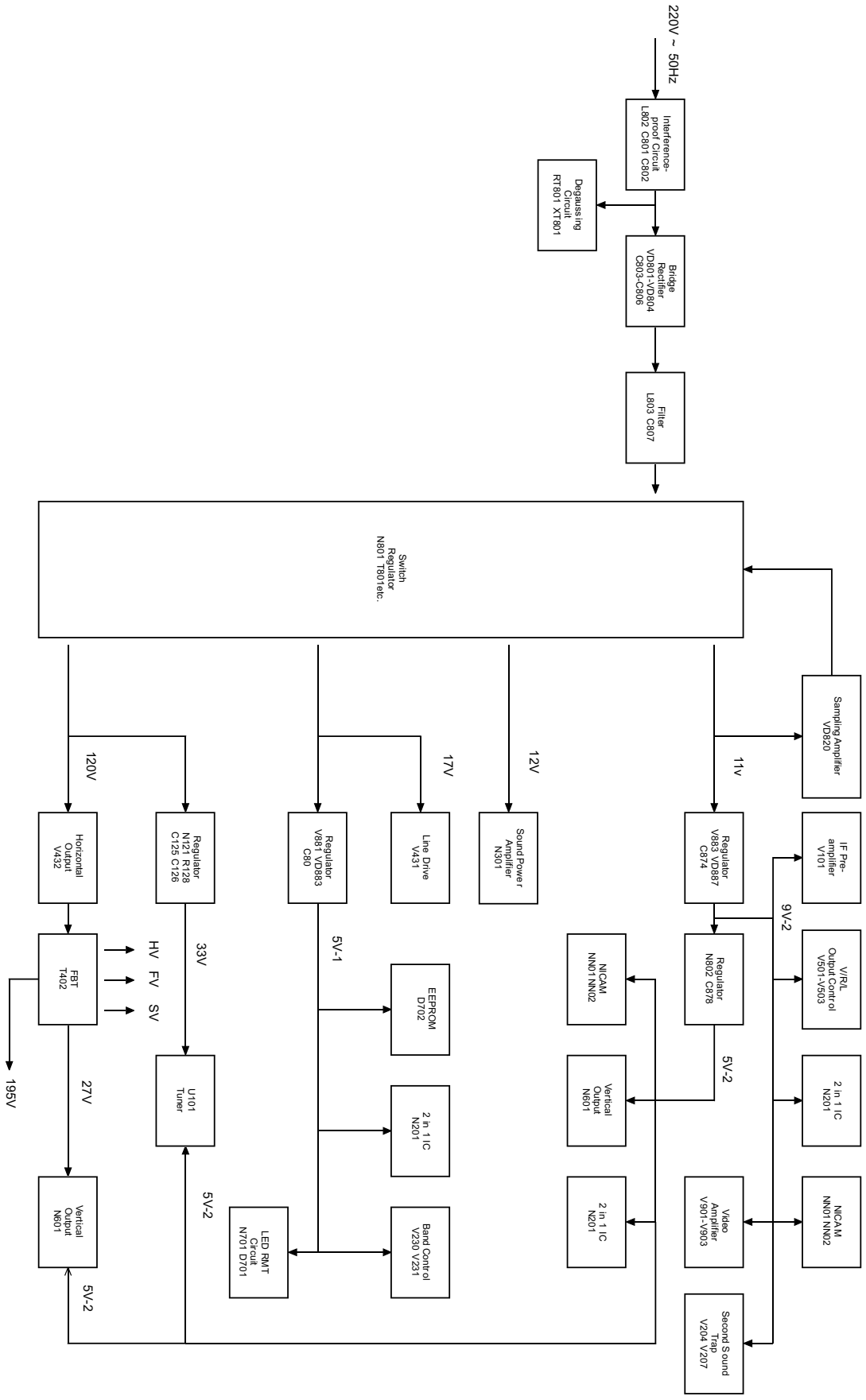


Fig. 11 Diagram for CN-18EA Supply Voltage System

3. CHASSIS DESCRIPTION

General Description

CN-18EA chassis is applied in 21E88 series. By use of Toshiba V/C/D-MCU 2IN1 IC for TV small signal processing and bus control, the chassis enables TV tuning, adjustment, control and picture correction, featuring high-integration, high-performance-to-price ratio and high-reliability and compact circuit with fewer external components. The chassis, widely used in small and medium TVs, provides much more convenience for manufacturing and technical service. It includes:

- 2IN1 IC TMAP8801PSBNG for PAL/NTSC/SECAM small signal processing and bus control
- EEPROM AT24C16 for data memory
- LA78040 for vertical output power amplifying
- TDA8944J (stereo)/TDA8943SF (mono) for audio power amplifying
- TDA9808T combined with MSP3410G into NICAM/IGR demodulator
- Thick-film IC STR-G5653 for power circuit adjustment and control

The following features are available in the chassis:

- Color systems: PAL/NTSC/SECAM
- Sound systems: D/K B/G I M
- 236 programs preset
- Multilingual on screen display
- I^2C bus control
- NICAM/IGR/AV stereo
- Selectable picture/sound modes
- Intelligent lock
- Message board
- Telephone directory
- Game
- Biorhythm
- Calendar inquiry

The chassis mainly uses the following ICs and assemblies.

Table 5 Key ICs and Assemblies

Serial No.	Position	Type	Description
1	D702	AT24C16	EERPOM
2	N201	TMPA8801PSBNG	2IN1 IC (Small signal processor + micro control unit (MCU))
3	N301	TDA8943SF/TDA8944J	Audio power amplifier
4	N601	LA78040	Vertical scan output stage circuit
5	N801	STR-G5653	Switch-mode power supply control
6	NN01	TDA9808T	Audio IF demodulator
7	NN02	MSP3410G	NICAM audio processor
8	U101	TDQ-5B6M	Tuner

SERVICE DATA

TECHNICAL DATA OF KEY ICS

1. TOSHIBA 2IN1 IC SERIES

1) General Description

Toshiba 2IN1 IC series are super ICs combined small signal processing with 8-bit micro control unit, including TMPA8801/8802/8803/8807/8808/8809/8812/8813/8821/8823/ 8827/8829 with the following features.

Table 6

Type	Type (for ICs with OTP ROM)	Color System	ROM	E/W Correction	Package
TMPA8801CSBNG/ CPBNG/CMBNG	TMPA8801PSBNG	PAN/NTSC/SECAM	64K/48K/32K		SDIP64
TMPA8802CSBNG/ CPBNG/CMBNG	TMPA8801PSBNG	NTSC	64K/48K/32K		SDIP64
TMPA8803CSBNG/ CPBNG/CMBNG	TMPA8801PSBNG	PAN/NTSC	64K/48K/32K		SDIP64
TMPA8801CSCNG/ CPCNG/CMCNG	TMPA8801PSCNG	PAN/NTSC/SECAM	64K/48K/32K		SDIP64
TMPA8807CSBNG/ CPBNG/CMBNG	TMPA8807PSBNG	PAN/NTSC/SECAM	64K/48K/32K	Yes	SDIP64
TMPA8808CSBNG/ CPBNG/CMBNG	TMPA8807PSBNG	NTSC	64K/48K/32K	Yes	SDIP64
TMPA8809CSBNG/ CPBNG/CMBNG	TMPA8807PSBNG	PAN/NTSC	64K/48K/32K	Yes	SDIP64
TMPA8813CSNG/ CPNG/CMNG	TMPA8813PSNG	PAN/NTSC	64K/48K/32K		SDIP64
TMPA8821CSNG/ CPNG/CMNG	TMPA8821PSNG	PAN/NTSC/SECAM	64K/48K/32K		SDIP64
TMPA8823CSNG/ CPNG/CMNG	TMPA8821PSNG	PAN/NTSC	64K/48K/32K		SDIP64
TMPA8827CSNG/ CPNG/CMNG	TMPA8827PSNG	PAN/NTSC/SECAM	64K/48K/32K	Yes	SDIP64
TMPA8829CSNG/ CPNG/CMNG	TMPA8827PSNG	PAN/NTSC	64K/48K/32K	Yes	SDIP64
TMPA8812CSDNG/ CPDNG/CMDNG	TMPA8812PSDNG	NTSC	64K/48K/32K	Yes	SDIP56

TMPA8801/8807PSBNG is applied in the chassis as an important TV signal processing chip.

TMPA8801/8807CMBNG /CPBNG/CRBNG /CSBNG

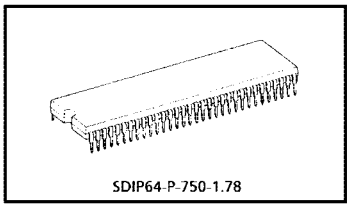
MCU AND SIGNAL PROCESSOR FOR A PAL/NTSC/SECAM TV

The TMPA8801/8807CMBNG /CPBNG /CRBNG /CSBNG is an integrated circuit for a PAL/NTSC/SECAM TV. A MCU and a TV signal processor are integrated in a 64-pin shrink DIP package. The MCU contains 8-bit CPU, ROM, RAM, I/O ports, timer/counters, A/D converters, an on-screen display controller, remote control interfaces, IIC bus interfaces and the Closed Caption decoder. The TV signal processor contains PIF, SIF, Video, multi-standard chroma, Sync, RGB processors.

MROM: TMPA8801/8807CMBNG (ROM: 32k)
TMPA8801/8807CPBNG (ROM: 48k)
TMPA8801/8807CRBNG (ROM: 56k)
TMPA8801/8807CSBNG (ROM: 64k)

OTP: TMPA8801/8807PSBNG ROM size 64k

Weight: 8.85 g (typ.)



Weight: 8.85 g (typ.)

Fig. 12

2). Features

MCU

- High speed 8-bit CPU (TLCS-870/X series)
- Instruction execution time: 0.5 s (at 8 MHz)
- (TMPA8801/8807CMBNG)
  32-Kbytes ROM, 2-Kbytes RAM
  (TMPA8801/8807CPBNG)
  48-Kbytes ROM, 2-Kbytes RAM
  (TMPA8801/8807CRBNG)
  56-Kbytes ROM, 2-Kbytes RAM
  (TMPA8801/8807CSBNG)
  64-Kbytes ROM, 2-Kbytes RAM
- ROM correction
- 12 I/O ports
- 14-bit PWM output 1 ch for a voltage synthesizer
- 7-bit PWM output 1 chan
- 8-bit A/D converter 3 ch for a touch-key input with key ON wake-up CIRCUIT
- Remote control signal preprocessor
- Two 16-bit internal timer/counter 2 ch
- Two 8-bit internal timer/counter 2 ch
- Time base timer, watchdog timer
- 16 interrupt sources: external 5, internal 11
- IIC bus interface (multi-master)
- STOP and IDLE power saving modes

TV Processor

IF

- Integrated PIF VCO aligned automatically
- Negative demodulation PIF
- Multi-frequency SIF demodulator without external Tank-coil

Video

- Integrated chroma traps
- Black stretch
- Y-gamma

Chroma

- Integrated chroma BPFs
- PAL/NTSC/SECAM demodulation

CCD Decoder

- Digital data slicer for NTSC

OSD

- Clock generation for OSD display
- Font ROM characters: 384 characters
- Characters display: 32 columns × 12 lines
- Composition: 16 × 18 dots
- Size of character: 3 (line by line)
- Color of character: 8 (character by character)
- Display position: H 256/V 512 steps
- BOX function
- Fringing, smoothing, Italic, underline function
- Conform to CCD REGULATION
- Jitter elimination

RGB/Base-Band

- Integrated 1 H base-band delay line
- Base-band TINT control
- Internal OSD interface
- Half-tone and transparent for OSD
- External YCbCr interface for DVD
- RGB cut-off/drive controls by bus
- ABCL (ABL and ACL combined)

Sync.

- Integrated fH ×640 VCO
- DC coupled vert. ramp output (single)
  EW correction with EHT input **(For TMPA8807 Only)**

AV Switch (For TMPA8801 Only)

- 1 for video and 1 for audio (monaural)

3). Block Diagram for TMPA8801

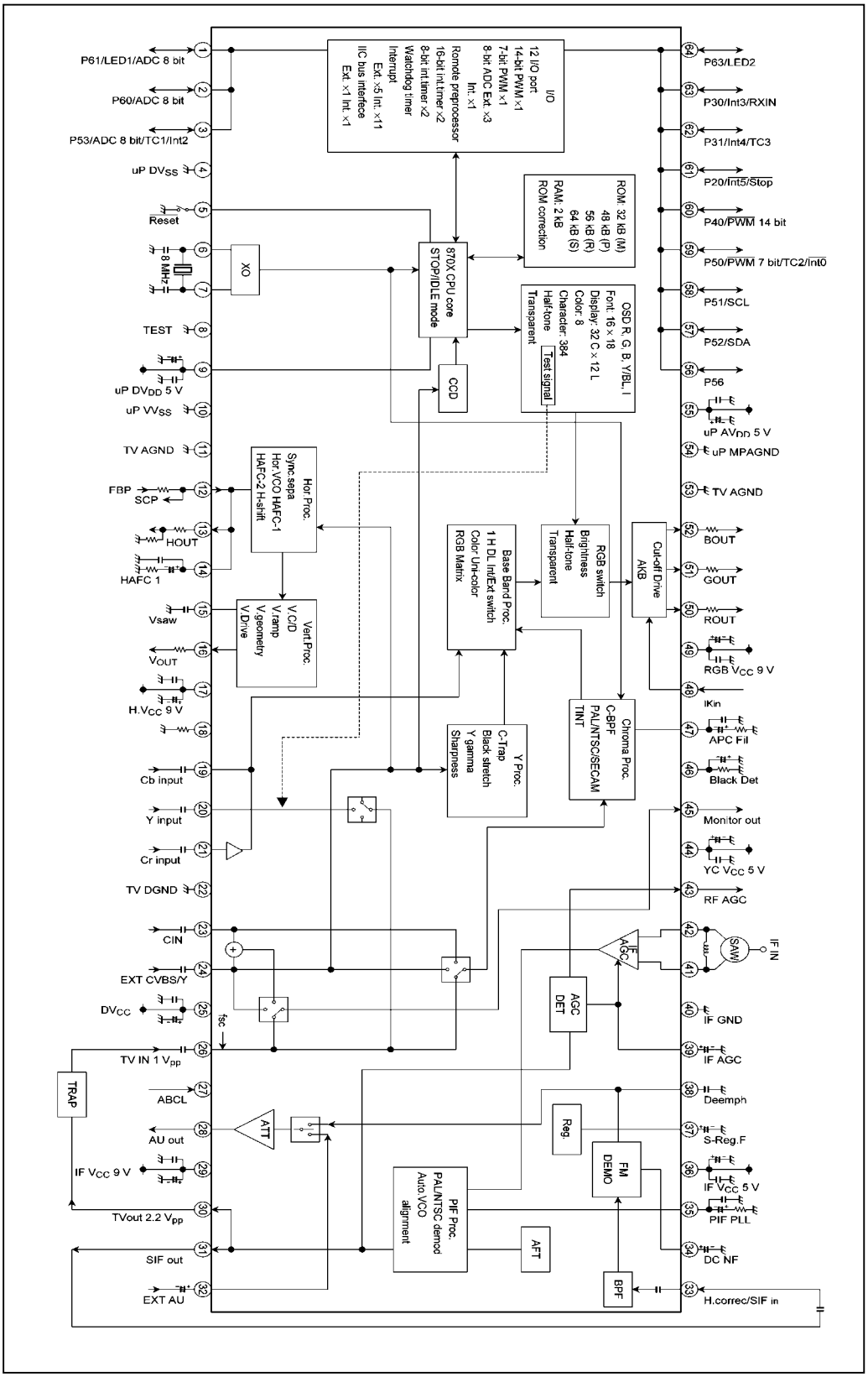


Fig. 13

4). Block Diagram for TMPA8807

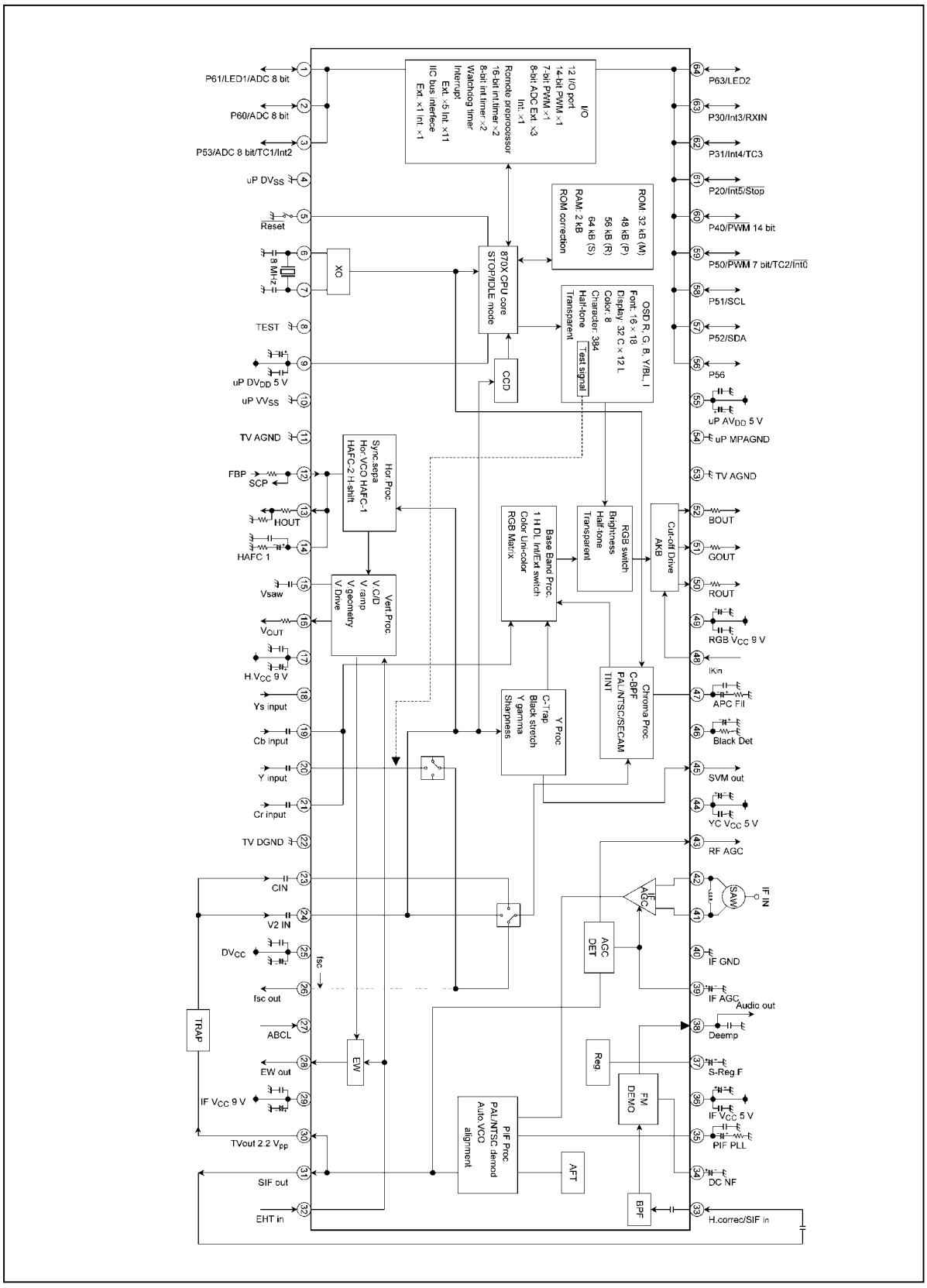


Fig. 14

5). Basic Structure

5.1). Internal Connections

TMPA8801/8807 has two pieces of IC chip in one package, using Multi-Chip-Package (MCP) technology. One is
a micro controller (MCU) and the other one is a signal processor (SP) for a color TV. There are some internal connections between these two ICs for handling below signals.

Table 7 Signal Name Direction Description

	Signal Name	Direction	Description
1	SCL	M to S	Internal IIC bus SCL
2	SDA	Bi-direction	Internal IIC bus SDA
3	OSD R	M to S	OSD signal connection
4	OSD G	M to S	OSD signal connection
5	OSD B	M to S	OSD signal connection
6	OSD Y/BL	M to S	OSD display control
7	OSD I, CS OUT	M to S	OSD half-tone control/Test pattern signal
8	C-Video	S to M	Composite video signal from internal video switch, for CCD
9	C-Sync	S to M	Composite sync. signal from sync. Separator, for CCD
10	HD	S to M	Horizontal timing pulse regenerated from FBP, for OSD
11	VD	S to M	Vertical timing pulse from sync. Separator, for OSD
12	CLK	M to S	8 MHz clock
13	AVDD	M to S	Reference voltage for C-Video interface
14	ADC	S to M	A/D converter monitoring RF-AGC, R-Y and B-Y

Functions of SP from MCU are controllable through the IIC bus of the internal connections.

5.2). Power Supply

TMPA8801/8807 has some power supplys and GND pins. Power supplies related MCU must be applied at the
first. Power supplies for H.VCC and TV D.VCC are the second with at least 100 ms delay after MCU power
ON. The other power supplies are the last, which are recommended to be supplied from a regulator circuit
using FBP.

5.3). Crystal Resonator

TMPA8801/8807 requires only one crystal resonator, in stead that a conventional two-chip solution requires
two resonators at least, one for MCU and the other one for SP. An oscillation clock with the crystal resonator of TMPA8801 /8807is supplied for MCU operation, PIF VCO automatic alignment, alignment free AFT,
chroma demodulation and horizontal oscillation. The oscillation frequency is very important so that those

of functions work properly, so that designing the oscillation frequency accurately is required. The spec of
crystal is recommended to be within
fosc: 8 MHz +/-20 ppm
ftemp: 8 MHz +/-40 ppm (-20°C to +65°C)
While RESET of MCU is active, the MCU function stops. Hardware and software initialization sequence including power supplies control is required, because status of any hardware after the RESET period is unknown especially horizontal oscillator which is a very basic timing generator of SP operation.

6).Terminal Interface

MCU Block

Table 8

Pin No.	Pin Name Interface Ci	I/O	Function
1	P61/LED1/ADC 8 bit (/KWU5) (AIN5) (LED1)	I/O (input) (input) (output)	 Key on wake up input A/D converter analog input High current sink open drain output
2	P60/ADC 8 bit (/KWU4) (AIN4)	I/O (input) (input)	 Key on wake up input A/D converter analog input
3	P53/ADC 8 bit/TC1/Int2 (/KWU0) (AIN0) (TC1) (INT2)	I/O (input) (input) (input) (input)	 Key on wake up input A/D converter analog input Timer/counter input External interrupt input
4	uP DVSS	Power Supply	GND
5	/Reset	I/O	Reset signal input or watchdog timer output Address trap reset output
6 7	XOUT XIN	Output Input	X'tal connecting pins
8	TEST	Input	Test pin for out-going test. Be tied to low.
9	uP DVDD 5 V	Power Supply	VDD Supply 5 V
10	uP VVSS	Power Supply	GND for Slicer circuit
54	uP MPAGND	Power Supply	GND for Oscillator circuit

(continued)

55	uP AVDD 5 V	Power Supply	VDD for OSD Oscillator circuit Supply 5 V
56	P56	I/O	
57	P52/SDA (SDA)	I/O (I/O)	 IIC bus serial data input/output
58	P51/SCL (SCL)	I/O (I/O)	 IIC bus serial clock input/output
59	P50/PWM 7 bit/TC2/ Int0 (/PWM8) (TC2) (/INT0)	I/O (output) (input) (input)	 7-bit D/A conversion (PWM) output Timer/Counter input External interrupt input
60	P40/PWM 14 bit (/PWM0)	I/O (output)	 14/12-bit D/A conversion (PWM) output
61	P20/Int5/Stop (/INT5) (/STOP)	I/O (input) (input)	 External interrupt input STOP mode release signal input
62	P31/Int4/TC3 (INT4) (TC3)	I/O (input) (input)	 External interrupt input Timer/Counter input
63	P30/Int3/RXIN (INT3) (RXIN)	I/O (input) (input)	 External interrupt input Remote control signal Preprocessor input
64	P63/LED2/ (LED2)	I/O (output)	 High current sink open drain output

Signal Processor Block

Table 9

Pin No.	Pin Name	Function
11	TV AGND	GND terminal for Analog block.
12	FBP in	Input terminal for FBP.
13	HOUT	Output terminal for Horizontal driving pulse.
14	HAFC 1	Terminal to be connected capacitor for HAFC filter. This terminal voltage controls H VCO frequency.

(continued)

15	V saw	Terminal to be connected capacitor to generate V saw signal. V saw amplitude is kept constant by V AGC function.
16	V OUT	Output terminal for Vertical driving pulse.
17	H.VCC 9 V	VCC terminal for DEF circuit. Supply 9 V.
18	-(For TMPA8801)	Connect to GND via resister
	YS in (For TMPA8807)	Terminal for switching of PIP mode PIP signal (YUV input) 1.75V Main signal (TV/EXT/YC) GND Ys voltage
19	Cb input	Input terminal for Cb signal.
20	Y input	Input terminal for Y signal. (Input level =1 Vp-p
21	Cr input	Input terminal for Cr signal. It is recommended that input impedance is low.
22	TV DGND	GND terminal for Digital block.
23	CIN	Input terminal for Chroma signal.
24	EXT CVBS/Y (V2 IN)	Input terminal for Video signal. (Input level =1 Vp-p)
25	TV DVCC	VCC terminal for Digital block. This terminal voltage is clipped about 3.3 V by regulator circuit. Supply TV DVCC voltage from HVCC (#17) voltage via 27Ω.
26	TV IN (V1 in) (For TMPA8801)	Input terminal for Video signal. (Input level =1 Vp-p)
	fsc out (For TMPA8807)	Output terminal for fsc wave signal. (Output level =0.55Vp-p typ.)
27	ABCL	Input terminal for ABL/ACL control.
28	AU out (For TMPA8801)	Output terminal for Audio signal.
	Ew out (For TMPA8807)	Output terminal for East-West correction signal.
29	IF VCC 9 V	VCC terminal for IF circuit. Supply 9 V.
30	TVout	Output terminal for detected PIF signal. (Output level =2.2 Vp-p)
31	SIF out	Output terminal for detected SIF signal.
32	EXT AU in (For TMPA8801)	Input terminal for External Audio signal.
	EXT in (For TMPA8807)	Input terminal for EHT feedback signal.
33	H.correc/SIF in	Input terminal for H correction and 2nd SIF.
34	DC NF	Terminal to be connected capacitor for DC Negative Feedback from SIF Det output.
35	PIF PLL	Terminal to be connected with loop filter for PIF PLL. This terminal voltage is controlled PIF VCO frequency.

(continued)

36	IF VCC 5 V	VCC terminal for IF circuit. Supply 5 V.
37	S-Reg.F	Terminal to be connected capacitor for stabilizing internal bias.
38	Deemph/ Audio out	Terminal to be connected capacitor for SIF Det De-Emphasis.
39	IF AGC	Terminal to be connected with IF AGC filter.
40	IF GND	GND terminal for IF circuit.
41 42	IF IN	Input terminals for IF signals. Pin 41 and Pin 42 are both input poles of differential amplifier.
43	RF AGC	Output terminal for RF AGC control level.
44	YC VCC 5 V	VCC terminal for Y/C circuit. Supply 5 V.
45	Monitor out	Output terminal for CVBS or Y signal selected by BUS (video SW).
46	Black Det	Terminal to be connected with Black Det filter for black stretch.
47	APC Fil (Chrome PLL filter)	Terminal to be connected with APC filter for Chroma demodulation. This terminal voltage controls frequency of VCXO.
48	IKin	Input terminal to sense AKB cathode current.
49	RGB VCC 9 V	VCC terminal for RGB circuit. Supply 9 V.
50	ROUT	Output terminal for R signal.
51	GOUT	Output terminal for G signal.
52	BOUT	Output terminal for B signal.
53	TV AGND	GND terminal for Analog block.

7). Microcontrollers Descriptions (MROM version: TMPA8801/8807CMBNG /CPBNG /CRBNG /CSBNG)

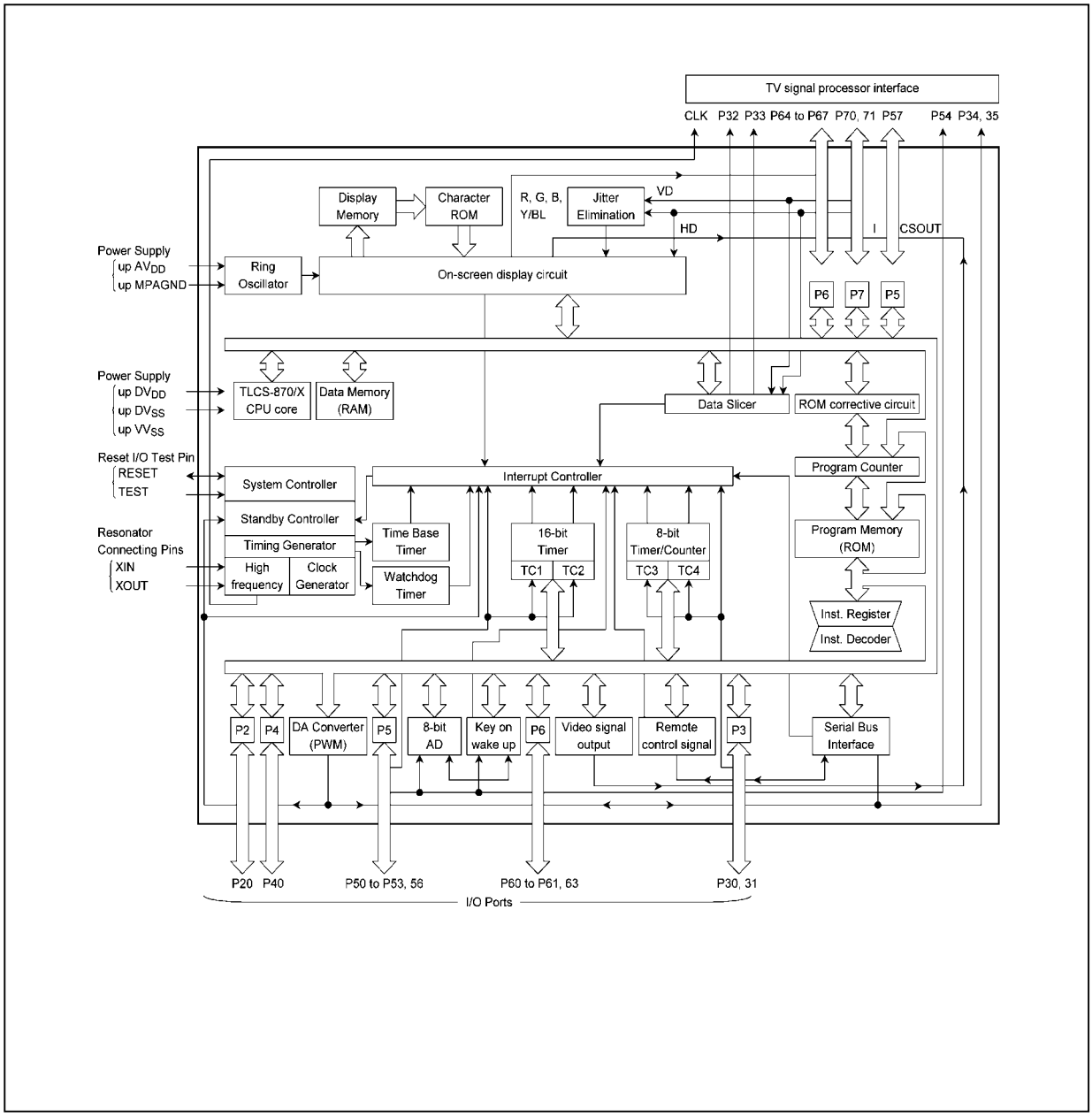


Fig. 15

2. AUDIO POWER AMPLIFIER TDA8943SF/TDA8944J
6 W MONO BRIDGE TIED LOAD (BTL) AUDIO AMPLIFIER

1). General description

The TDA8943SF is a single-channel audio power amplifier with an output power of 6 W at an 8 Ω load and a 12 V supply. The circuit contains a Bridge Tied Load (BTL) amplifier with an all-NPN output stage and standby/mute logic. The TDA8943SF comes in a 9-lead single in-line (SIL) medium power package. The TDA8943SF is printed-circuit board (PCB) compatible with all other types in the TDA894x family. One PCB footprint accommodates both the mono and the stereo products.

2). Features

Few external components

- ❷ Fixed gain
- ❷ Standby and mute mode
- ❷ No on/off switching plops
- ❷ Low standby current
- ❷ High supply voltage ripple rejection
- ❷ Outputs short-circuit protected to ground, supply and across the load
- ❷ Thermally protected
- ❷ Printed-circuit board compatible.

3). Block diagram

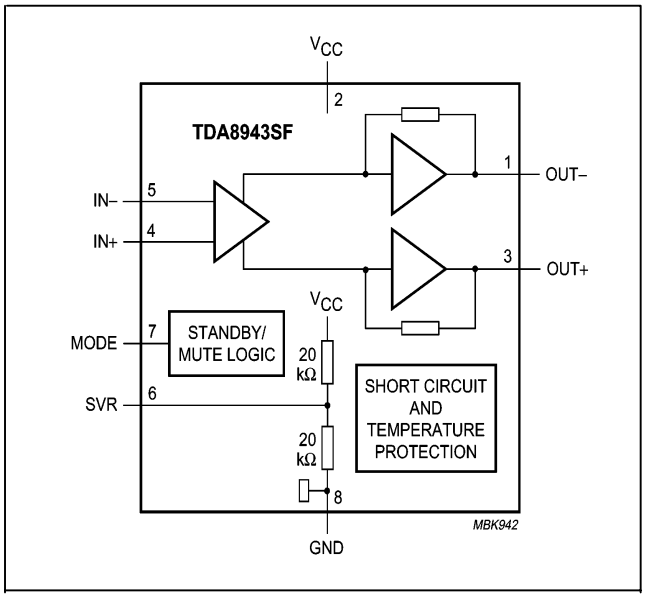


Fig. 16

4). Pinning information

4.1) Pinning

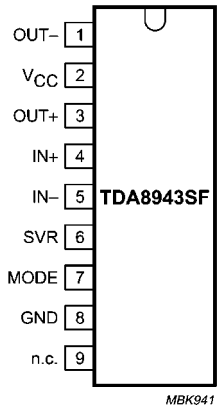


Fig 17. Pin configuration.

4.2) Pin description

Table 10 Pin description

Symbol	Pin	Description
OUT–	1	negative loudspeaker terminal
VCC	2	supply voltage
OUT+	3	positive loudspeaker terminal
IN+	4	positive input
IN–	5	negative input
SVR	6	half supply voltage decoupling (ripple rejection)
MODE	7	mode selection input (standby, mute, operating)
GND	8	ground
n.c.	9	not connected

TDA8943SF:Mono Bridge Tied Load (BTL) audio amplifier, Max output power:6W

3. TDA8944J

2 X 7 W STEREO BRIDGE TIED LOAD (BTL) AUDIO AMPLIFIER

1). General description

The TDA8944J is a dual-channel audio power amplifier with an output power of 2×7 W at an 8 Ω load and a 12 V supply. The circuit contains two Bridge Tied Load (BTL) amplifiers with an all-NPN output stage and standby/mute logic. The TDA8944J comes in a 17-pin DIL-bent-SIL (DBS) power package. The TDA8944J is printed-circuit board (PCB) compatible with all other types in the TDA894x family. One PCB footprint accommodates both the mono and the stereo products.

2). Features

- ❷ Few external components
- ❷ Fixed gain
- ❷ Standby and mute mode
- ❷ No on/off switching plops
- ❷ Low standby current
- ❷ High supply voltage ripple rejection
- ❷ Outputs short-circuit protected to ground, supply and across the load
- ❷ Thermally protected
- ❷ Printed-circuit board compatible.

3). Block diagram

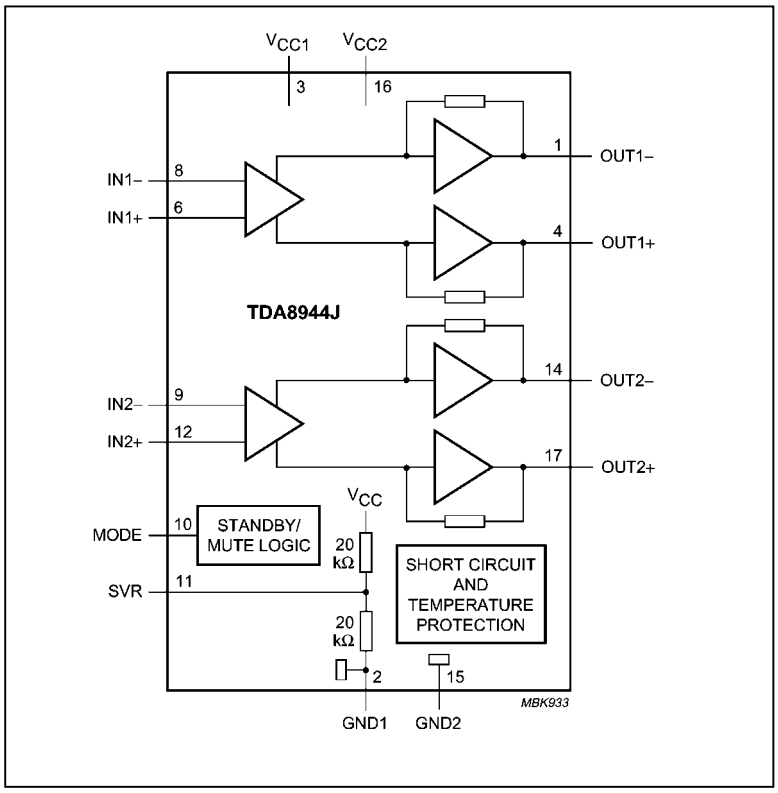


Fig 18. Block diagram.

4). Pinning information

4.1) Pinning

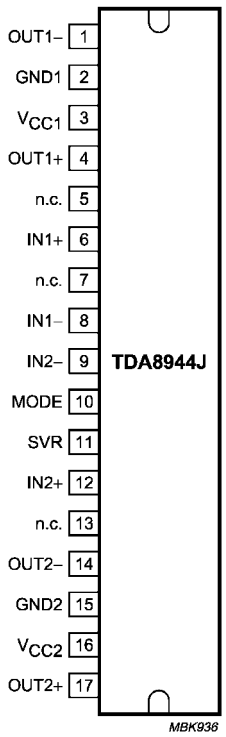


Fig 19. Pin configuration.

4.2) Pin description

Table 11 Pin description

Symbol	Pin	Description
OUT1−	1	negative loudspeaker terminal 1
GND1	2	ground channel 1
V_{CC1}	3	supply voltage channel 1
OUT1+	4	positive loudspeaker terminal 1
n.c.	5	not connected
IN1+	6	positive input 1
n.c.	7	not connected
IN1−	8	negative input 1
IN2−	9	negative input 2
MODE	10	mode selection input (standby, mute, operating)

(continued)

SVR	11	half supply voltage decoupling (ripple rejection)
IN2+	12	positive input 2
n.c.	13	not connected
OUT2−	14	negative loudspeaker terminal 2
GND2	15	ground channel 2
V_{CC2}	16	supply voltage channel 2
OUT2+	17	positive loudspeaker terminal 2

TDA8944J: Stereo power amplifier, Max output power: 2×7W

4. VERTICAL SCAN OUTPUT STAGE CIRCUIT LA78040/LA78041

Both LA78040/LA78041 are vertical scan output stage power amplifiers. But there is a little bit difference between the two amplifiers, that is, LA78040 has supply voltage of 24V and output current of 1.8A_{P-P} while LA78041 has supply voltage of 30V and output current of 2.2A_{P-P}.

LA78040 /LA78041

Vertical Deflection Output Circuit

1). Features

·Low power dissipation due to built-in pump-up circuit

·Vertical output circuit

·Thermal protection circuit built in

·Excellent crossover characteristics

DC coupling possible

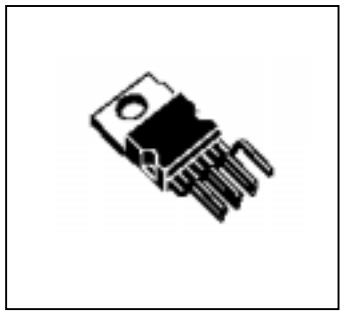


Fig. 20

2). Block Diagram

Package Type: TO-220-7H

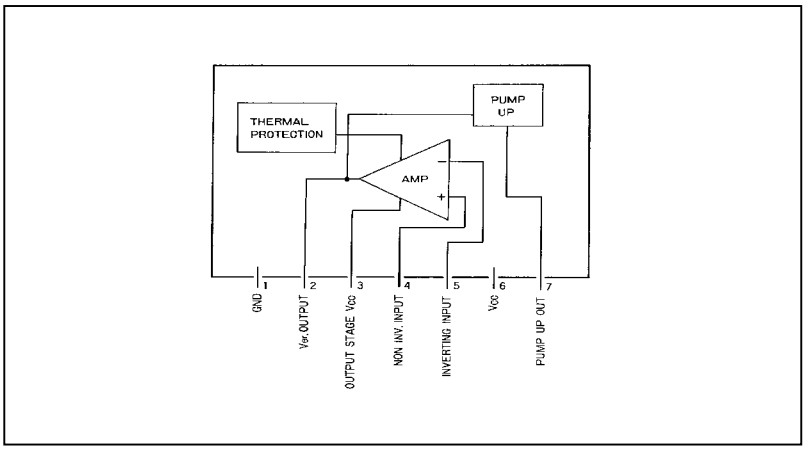


Fig.21

5. TDA9808T

SINGLE STANDARD VIF-PLL WITH QSS-IF AND FM-PLL DEMODULATOR

1). Features

·5V supply voltage (9V supply voltage for TDA9808T (DIP20) only)
·Applicable for IFs (Intermediate Frequencies) of 38.9MHz, 45.75MHz and 58.75 MHz
·Gain controlled wide band Video IF (VIF)-amplifier (AC-coupled)
·True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
·Robustness for over-modulation better than 105% due to Phase Locked Loop (PLL)-bandwidth control at negative modulated standards
·VIF Automatic Gain Control (AGC) detector for gain control, operating as peak sync detector
·Tuner AGC with adjustable TakeOver Point (TOP)
·Automatic Frequency Control (AFC) detector without extra reference circuit
·AC-coupled limiter amplifier for sound intercarrier signal
·Alignment-free FM-PLL demodulator with high linearity
·Sound IF (SIF) input for single reference Quasi Split
Sound (QSS) mode (PLL controlled); SIF AGC detector for gain controlled SIF amplifier, single reference QSS mixer for high performance
·Electrostatic Discharge (ESD) protection for all pins.

2). General Description

The TDA9808T is an integrated circuit for single standard (negative modulated) vision IF signal processing and FM demodulation, with single reference QSS-IF in TV and VTR sets.

3).Block Diagram

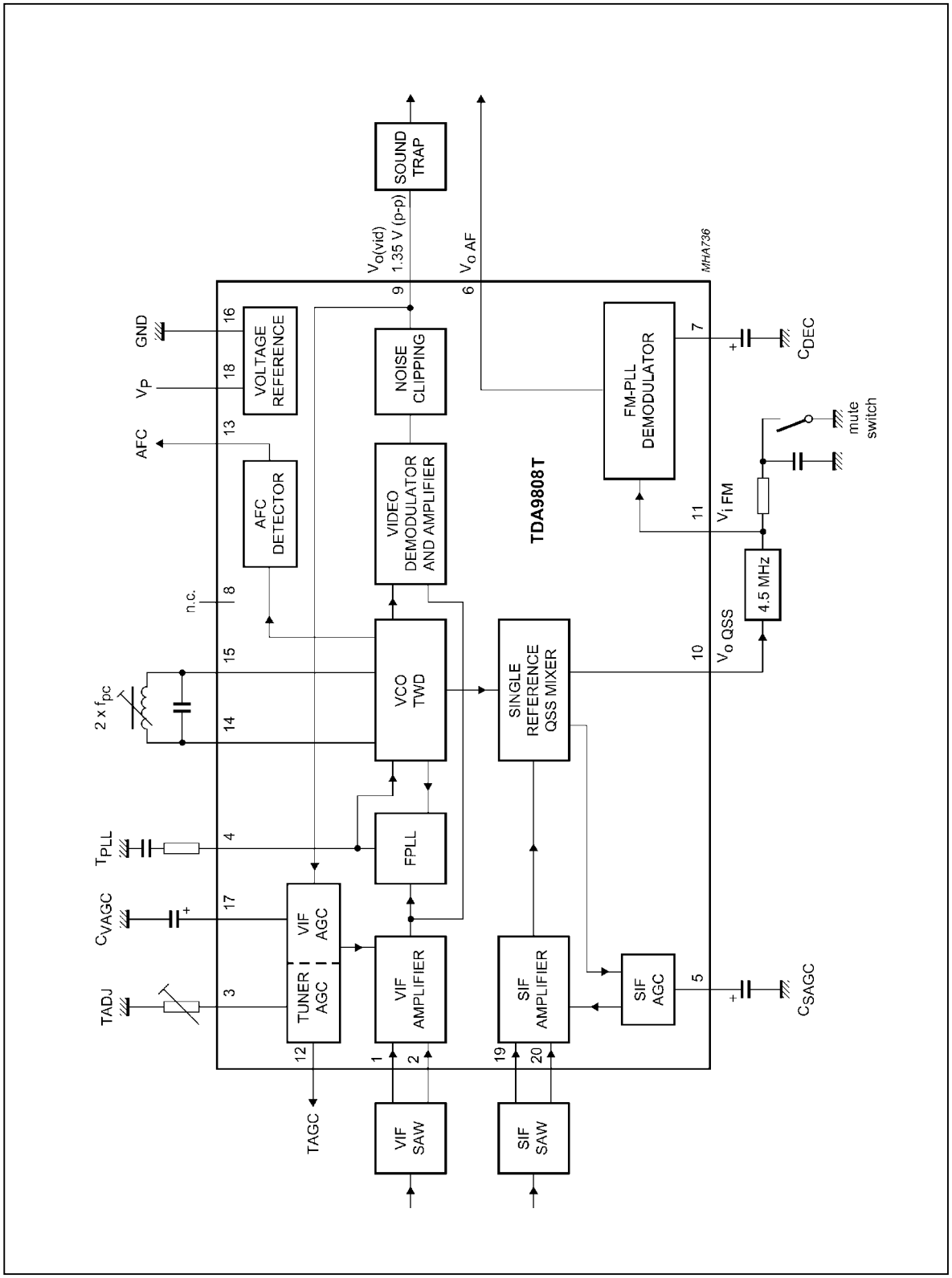


Fig. 22 Block Diagram

6. MSP34X0G
MULTISTANDARD SOUND PROCESSOR FAMILY

Release Note: Revision bars indicate significant changes to the previous edition. The hardware and software description in this document is valid for the MSP34X0G version B5 and following versions.

1). Introduction

The MSP34X0G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV-Standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed on a single chip. Figure 10 shows a simplified functional block diagram of the MSP34X0G.

This new generation of TV sound processing ICs now includes versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively MICRONAS Noise Reduction (MNR) is performed alignment free.

Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM Stereo Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J.
The MSP34X0G has optimum stereo performance without any adjustments.

All MSP34X0G versions are pin and software downward-compatible to the MSP34X0G. The MSP34X0G further simplifies controlling software. Standard selection requires a single I^2C transmission only.
The MSP34X0G has built-in automatic Functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/stereo/bilingual, no I^2C interaction is necessary (Automatic Sound Selection).

The ICs are produced in submicron CMOS technology.
The MSP34X0G is available in the following packages, PLCC68, PSDIP64, PSDIP52, PQFP80 and PLQFP64.

2). Block Diagram

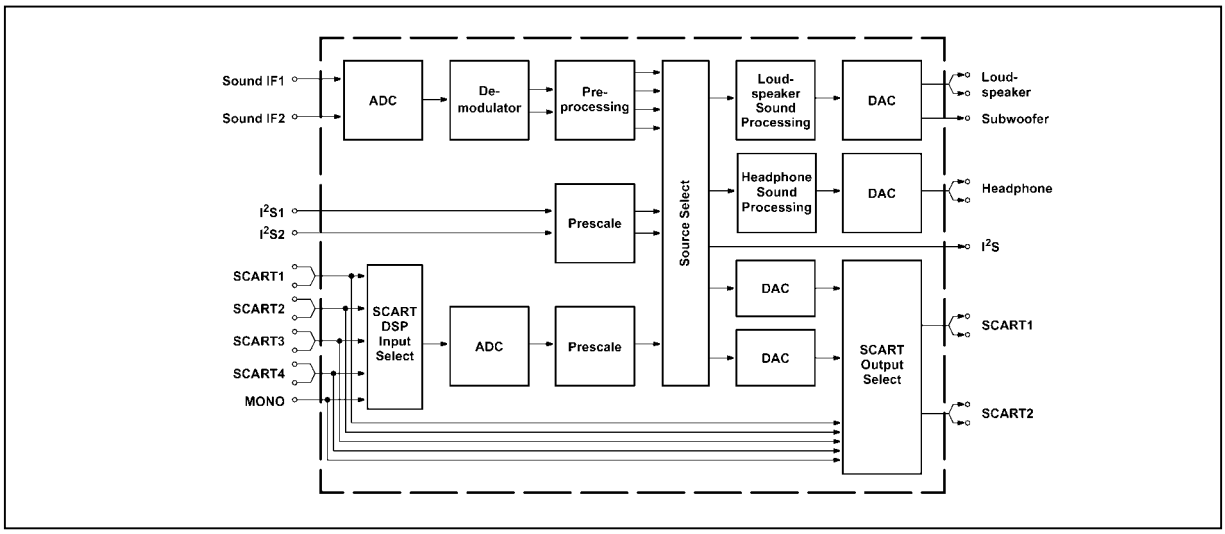


Fig. 23 Simplified Functional Block Diagram of the MSP34X0G

7．EEPROM AT24C04/08/16

1) Features

Low-voltage and Standard-voltage Operation

-2.7 (Vcc=2.7V to 5.5V)

-1.8 (Vcc=1.8V to 5.5V)

Internally Organized 128x8(1K), 256x8 (2K), 512x8 (4K),

1024x8 (8K) or 2048x8 (16K)

2-wire Serial Interface

Schmitt Trigger, Filtered Inputs for Noise Suppression

Bi-directional Data Transfer Protocol

100kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility

Write Protect Pin for Hardware Data Protection

8-byte Page (1K, 2K), 16-byte Page (4K, 8K, 16K) Write Modes

Partial Page Writes are Allowed

Self-timed Write Cycle (10 ms max)

High-reliability

-Endurance: 1 Million Write Cycles

- Data Retention: 100 Years

Automotive Grade and Extended Temperature Devices Available

8-lead PDIP, 8-lead JEDEC SOIC, 8-lead MAP and 8-lead TSSOP Package

2-wire

Serial EEPROM

AT24C01A 1K (128 x 8)

AT24C02 2K (256 x 8)

AT24C04 4K (512 x 8)

AT24C08 8K (1024 x 8)

AT24C16 6K (2048 x 8)

2) Description

The AT24C01A/02/04/08/16 provides 1024/2048/4096/8192/16384 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 128/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The AT24C01A/02/04/08/16 is available in space-saving 8-pin PDIP, 8-lead JEDEC SOIC, 8-lead MAP and 8-lead TSSOP packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 2.7V (2.7V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

3) Pin Configuration

Table 12

Pin Name	Function
A0-A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

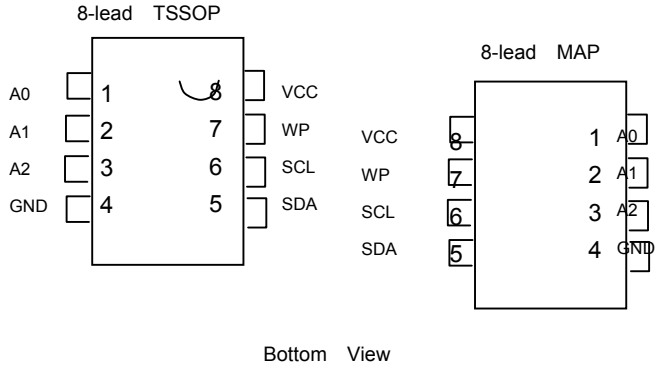


Fig. 24

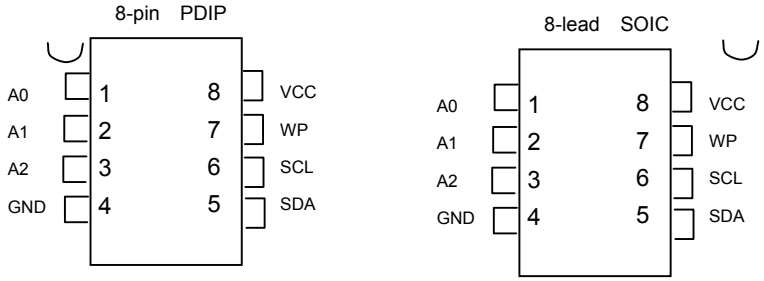


Fig.25

4) Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired for the AT24C01A and the AT24C02. As many as eight 1K/2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The AT24C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect.

The AT24C08 only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

The AT24C16 does not use the device address pins, which limits the number of devices on a single bus to one. The A0, A1 and A2 pins are no connects.

WRITE PROTECT (WP): The AT24C01A/02/04/16 has a Write Protect pin that provides hardware data

protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to Vcc, the write protection feature is enabled and operates as shown in table 13.

Table 13

WP Pin Status	Part of the Array Protected				
	24C01A	24C02	24C04	24C08	24C16
At Vcc	Full (1K) Array	Full (2K) Array	Full (4K) Array	Normal Read/ Write Operation	Upper Half (8K) Array
At GND	Normal Read/Write Operations				

5) Memory Organization

AT24C01A, 1K SERIAL EEPROM: Internally organized with 16 pages of 8 bytes each, the 1K requires a 7-bit data word address for random word addressing.

AT24C02, 2K SERIAL EEPROM: Internally organized with 32 pages of 8 bytes each, the 2K requires an 8-bit data word address for random word addressing.

AT24C04, 4K SERIAL EEPROM: Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

AT24C08, 8K SERIAL EEPROM: Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing.

AT24C16, 16K SERIAL EEPROM: Internally organized with 128 pages of 16 bytes each, the 16K requires an 11-bit data word address for random word addressing.

6) Block Diagram

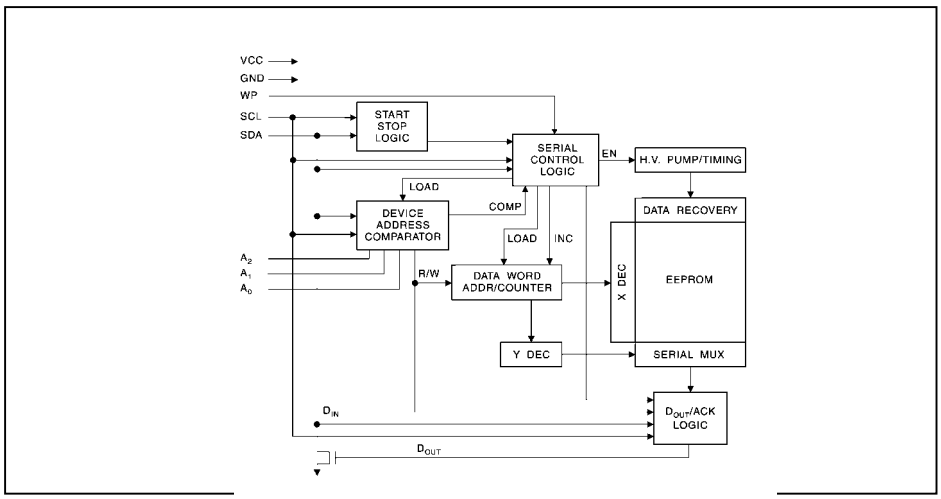


Fig.26

8. SWITCH-MODE POWER SUPPLY IC STRG5653/G8656

1). General Description

The STRG5653/G8656 are part of the STRG5600/G8600 series thick-film ICs for switch-mode power supply incorporating power MOSFET with a high-precise error amplifier. The ICs feature fewer external components, small-size and standard power supply.

The series STR-G8600 use Chip on Chip technology with the same operation principle as STR-G5600. Pin configuration, function and threshold of STR-G8600 are compatible with those of STR-G5600.

2) Block Diagram

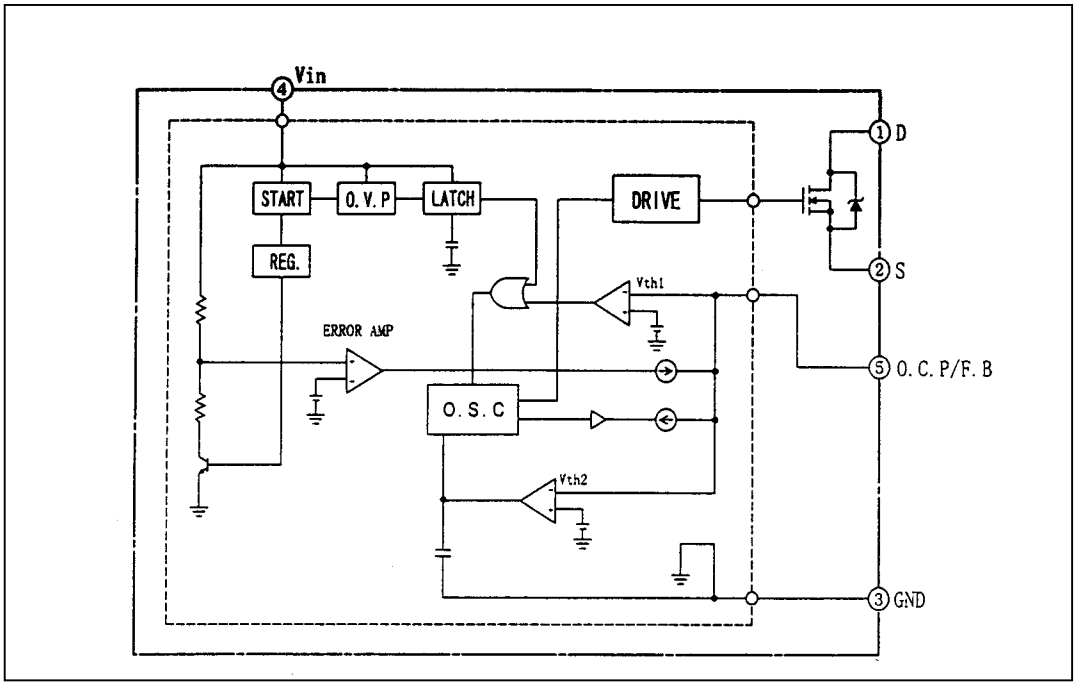


Fig.27

3).Function of Terminal

Table 14 Function of Terminal

Terminal No.	Symbols	Description	Functions
1	D	Drain Terminal	MOS FET drain
2	S	Source Terminal	MOS FET source
3	GND	Ground Terminal	Ground
4	VIN	Power supply Terminal	Input of power supply for control signals
5	O.C.P/F.B	Overcurrent/Feedback Terminal	Input of overcurrent detection signal and constant voltage signals

SERVICE DATA OF KEY ICS

Table 14 Functions and Service Data of AT24C08/16 Pins

Pin No.	Function Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (20KΩ)	Negative Resistance (20KΩ)
1	Address input	0	0.001	0.00
2	Address input	0	0.001	0.00
3	Address input	0	0.001	0.00
4	Common ground	0	0.001	0.00
5	Clock line	5	7	4.83
6	Data line	4.99	6.9	5.15
7	PW write protect	4.99	9.5	5.31
8	Supply voltage	5	3.5	3.25

Table 15 Functions and Service Data of MSP3410G Pins

Pin No.	Function Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (20KΩ)	Negative Resistance (20KΩ)
1	TP NC	0.16	7.3	5.3
2	AVD-GL-OUT NC	2.52	6.8	5.51
3	D-CTR-I/O-1 NC	0.01	7.3	5.57
4	D-CTR-I/O-0 NC	0.01	7.2	5.58
5	ADR-SEL	4.79	0.7	4.54
6	STANDBYQ	4.79	0.7	4.54
7	I2C-CL	3.56	7	4.44
8	I2C-DA	3.9	7	4.44
9	I2S-CL NC	2.36	7.2	6.24
10	I2S-WS NC	2.4	7.2	6.24
11	I2C-DA-WT NC	2.36	7.2	6.24
12	I2S-DA-IN1 NC	0.07	7.2	5.29
13	ADR-DA NC	0.07	7.2	5.59
14	ADR-WS	0.07	7.2	5.59
15	ADR-CL	0.07	7.2	5.59

(Continued)

16	DVSVP	4.79	0.7	4.54
17	DVSS	0.01	0.001	0.00
18	I2S-DA-IN2 NC	0.07	7.3	5.31
19	NC	0	∞	∞
20	RESETQ	4.76	7	5.24
21	DACA-R NC	0.8	3.5	3.54
22	DACA-L NC	0.08	3.5	3.52
23	VREF-I	0.01	0.001	0.00
24	DACM-R	0.17	3.5	3.52
25	DACM-L	0.08	3.5	3.54
26	DACM-SVB NC	0.18	3.6	3.6
27	SC2-OUT-R NC	3.82	7.1	5.92
28	SC2-OUT-L NC	3.82	7.1	5.91
29	CREF 1	0.01	0.001	0.00
30	SC1-OVT-R	3.82	7.1	5.91
31	SC1-OUT-L	3.82	7.1	5.92
32	SAPL-A	7.19	7.1	6.04
33	AHVSUP	8	1.3	4.59
34	CAPL-M	7.2	7.1	6.04
35	AHVSS	7.2	7.1	0.00
36	ABNDC	0.01	0.001	6.02
37	SC3-ZN-L NC	3.74	7.1	6.1
38	SC3-IN-R NC	3.77	7.1	6.1
39	SC2-IN-L NC	3.77	7.1	6.1
40	SC2-IN-R NC	3.77	7.1	6.1
41	SC1-IN-L	3.77	7.1	6.1
42	SC1-IN-R	3.77	7.1	6.1
43	VREFTOP	2.6	1.6	1.63
44	WONO-IN NC	3.78	7	6.1
45	AVSS	0.01	0.001	0.00
46	AVSVP	4.9	0.7	4.53
47	ANA-IN1+	1.53	7.3	5.27

(Continued)

48	ANA-IN1-	1.53	7.3	5.26
49	ANA-IN2+	0.09	7.3	5.27
50	TESTEN	0.01	0.001	0.00
51	XTAL-2N	2.35	6.8	5.27
52	XTAL-OUT	2.36Hs	6.8	5.3

Table 16 Functions and Service Data of TDA9808T Pins

Pin No.	Function Description	Digital Multimeter		
		Reference Voltage (V)	Positive Resistance (20KΩ)	Negative Resistance(20KΩ)
1	PIF signal input 1	3.23	7.2	6.03
2	PIF signal input 2	3.23	7.2	5.99
3	RFAGC start-control level adjust	0.99	6.7	5.85
4	PLL APC filter	2.53	7.9	6.3
5	Audio AGC filter	3.29	7.8	6.17
6	Audio output (NTSC 4.5MHz)	2.34	7.2	5.86
7	Filter	1.79	7.9	6.29
8	1/2VCC comparison voltage bias	0	∞	∞
9	Video output	2.18	7.6	6.09
10	Second SIF signal output	2.03	7.7	6.17
11	Second SIF signal input	2.81	5.2	4.99
12	RFAGC output	0.04		6.1
13	AGC signal output	3.05	7.9	6.2
14	External connection for VCO oscillating LC network	2.76	7	6
15	External connection for VCO oscillating LC network	2.76	7	6
16	Ground	0	0.001	0.00
17	AGC filter	3.13	7.9	6.11
18	Supply voltage input terminal	8	2.1	2.7
19	SIF signal input	3.2	2.1	6.27
20	SIF signal input?	3.2	7	6.27

Table 17 Ground Resistance of TMPA8801PSBNG Pins

Pin No	1	2	3	4	5	6
Resistance	31.70KΩ	31.70 KΩ	42.87 KΩ	0	5.5 KΩ	44.25 KΩ
Pin No	7	8	9	10	11	12
Resistance	44.31 KΩ	0	17.56 KΩ	0	0	39.79 KΩ
Pin No	13	14	15	16	17	18
Resistance	0.66 KΩ	39.81 KΩ	39.85 KΩ	10.55 KΩ	12.76 KΩ	24.70 KΩ
Pin No	19	20	21	22	23	24
Resistance	24.70 KΩ	24.67 KΩ	24.71 KΩ	0	0	24.62 KΩ
Pin No	25	26	27	28	29	30
Resistance	0.56 KΩ	24.70 KΩ	16.65 KΩ	22.04 KΩ	0.3 KΩ	3.27 KΩ
Pin No	31	32	33	34	35	36
Resistance	3.29 KΩ	24.27 KΩ	>2000 KΩ	362.3 KΩ	>2000 KΩ	0
Pin No	37	38	39	40	41	42
Resistance	20.1 KΩ	>2000 KΩ	>2000 KΩ	0	>2000 KΩ	>2000 KΩ
Pin No	43	44	45	46	47	48
Resistance	13.6 KΩ	0.5 KΩ	3.6 KΩ	223.3 KΩ	>2000 KΩ	0
Pin No	49	50	51	52	53	54
Resistance	0.5 KΩ	1217 KΩ	1396 KΩ	1352 KΩ	0	0
Pin No	55	56	57	58	59	60
Resistance	52 KΩ	60 KΩ	62 KΩ	60.8 KΩ	>2000 KΩ	>2000 KΩ
Pin No	61	62	63	64		
Resistance	56.6 KΩ	83 KΩ	80.9 KΩ			

Note: Measured when Power-off

Table 18 Operating Voltage of TMPA8801PSBNG (N201)'s Pins

1	2	3	4	5	6
5V	5V	5.2V	GND	5V	2.3V
7	8	9	10	11	12
2.3V	GND	5V	GND	GND	1V
13	14	15	16	17	18
1.6V	6V	4.2V	4.8V	8.4V	2.0V
19	20	21	22	23	24
2.4V	2.4V	2.4V	GND	0V	2.3V
25	26	27	28	29	30
3.4V	2.4V	4.8V	3.5V	9V	5V
31	32	33	34	35	36
1.8V	4.4V	2.8V	2.2V	2.5V	5V
37	38	39	40	41	42
2.2V	4.4V	4.2V	GND	1.7V	1.7V
43	44	45	46	47	48
4.2V	5V	1.2V	1.8V	2.5V	GND
49	50	51	52	53	54
9V	2.5V	2.5V	2.5V	GND	GND
55	56	57	58	59	60
5V	0V	5V	5V	5V	4.9V
61	62	63	64		
4.1V	5V	5V	0V		

Table 19 Functions and Service Data of LA78040/78041 Pins

Pin No.	Function Description	GDM8145 Multimeter		
		Voltage of Pin (V)	Ground Resistance (KΩ)	
			Measure with red probe while grounding black probe.	Measure with black probe while grounding red probe.
1	Ground	0	0	0
2	Vertical output terminal	9.73	0.58	0.58
3	Pump supply voltage input	24.88	∞	∞
4	In-phase input terminal	2.22	1.30	1.30
5	Inverting input terminal	2.22	4.58	4.55
6	Supply voltage	24.13	1.55	1.55
7	Pump supply voltage output/vertical flyback pulse output	2.61	7.09	5.93

REPLACEMENT OF PARTS

1. DESCRIPTION

Many electrical and mechanical components in this chassis have special safety-related characteristics. Components which have these special safety characteristics in this manual and its supplements are identified by the international hazard symbols or UL, FCC, FDA or VDE marking on the circuit diagram and parts list. When replacing any of these components, substitute the one which has the same safety characteristics as specified in the manual.

Description of the special markings:

A: The components identified by the A marking have special safety-related characteristics.

AE: The components identified by the AE marking are listed by EMC and have special safety-related characteristics.

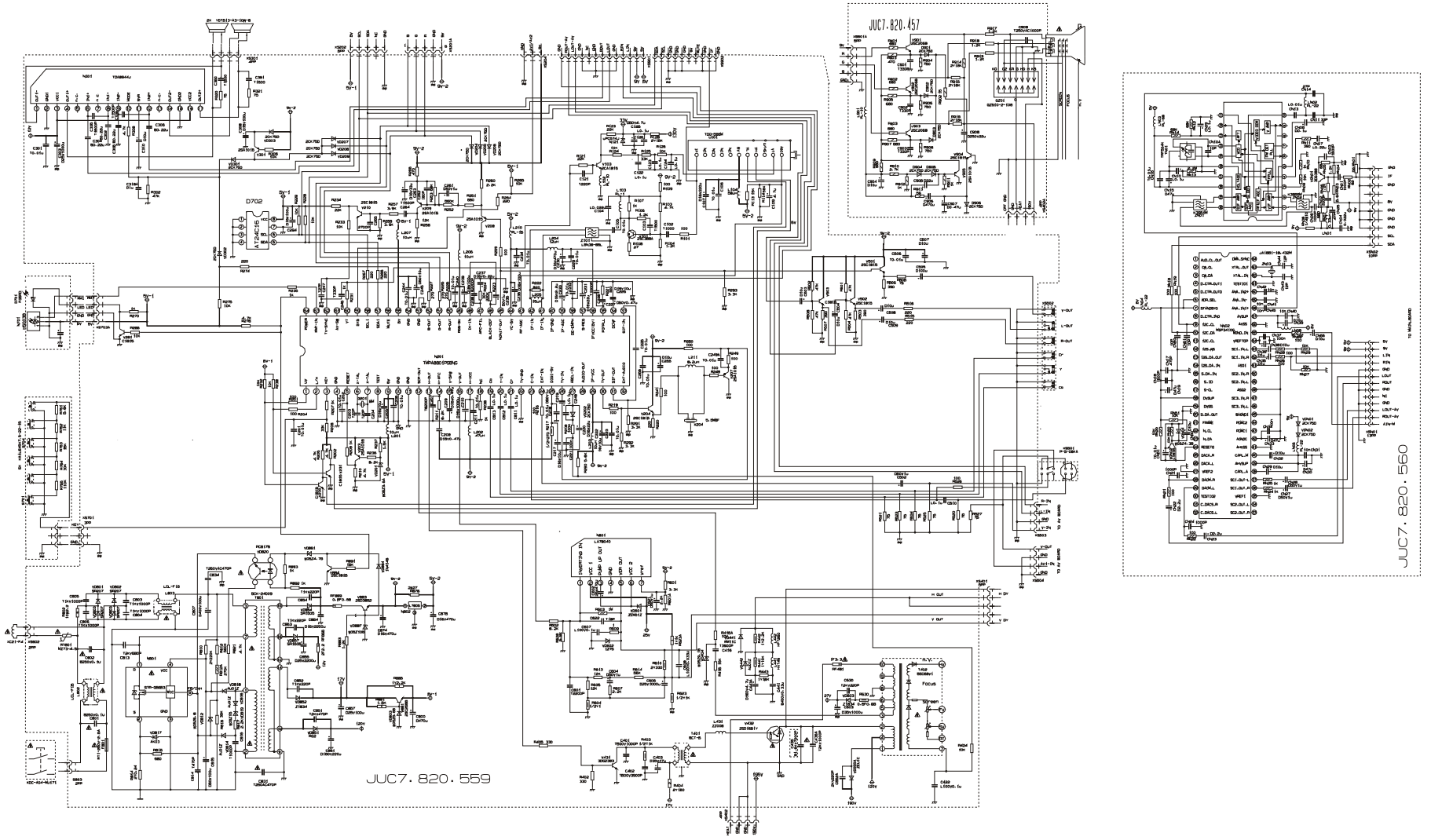
CB: The components identified by the CB marking have been evaluated to the CB standard.

E: The components identified by the E marking are listed by EMC

G: The components identified by the G marking have critical characteristics.

Z: The components identified by the Z marking have important characteristics.

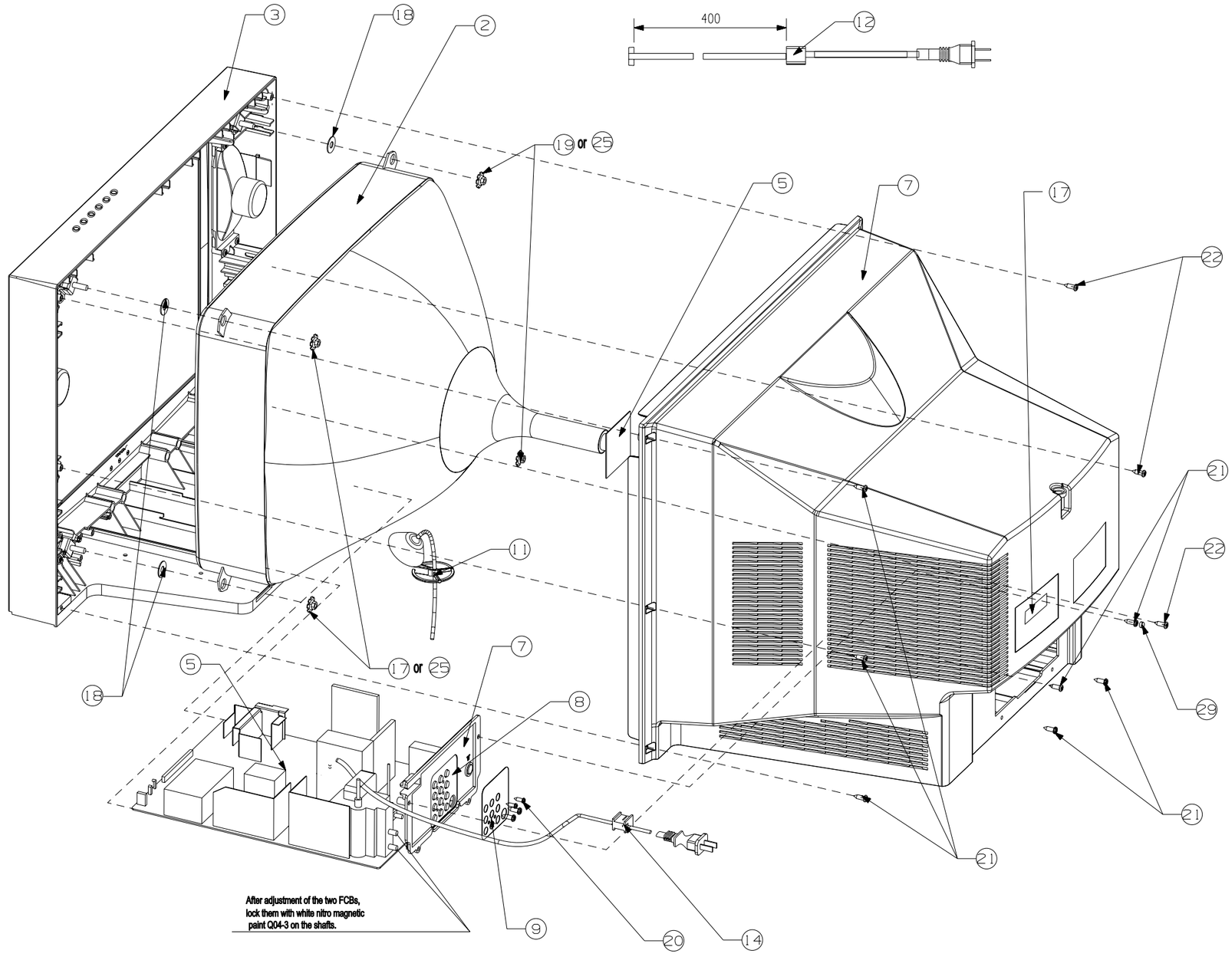
CIRCUIT DIAGRAM FOR 21E88



This circuit diagram is only for reference.
Specification are subject to change without notice.

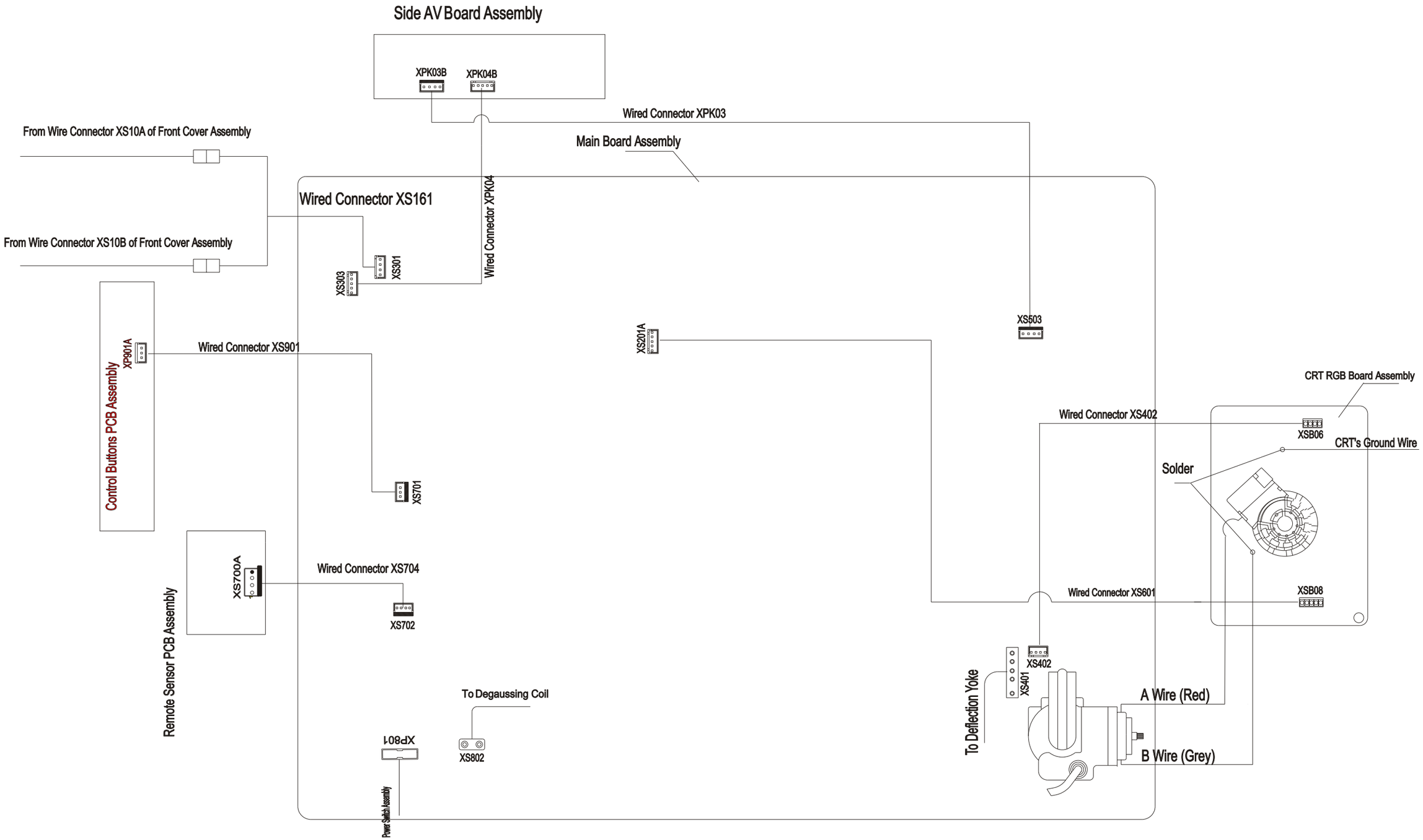
1. Any components identified by ⚠ have special safety-related characteristics.
   Use replacement components which have the same characteristics as the original parts.
2. ⏚ Cold ground ⊥ Hot ground

Final Assembly Diagram for 21E88

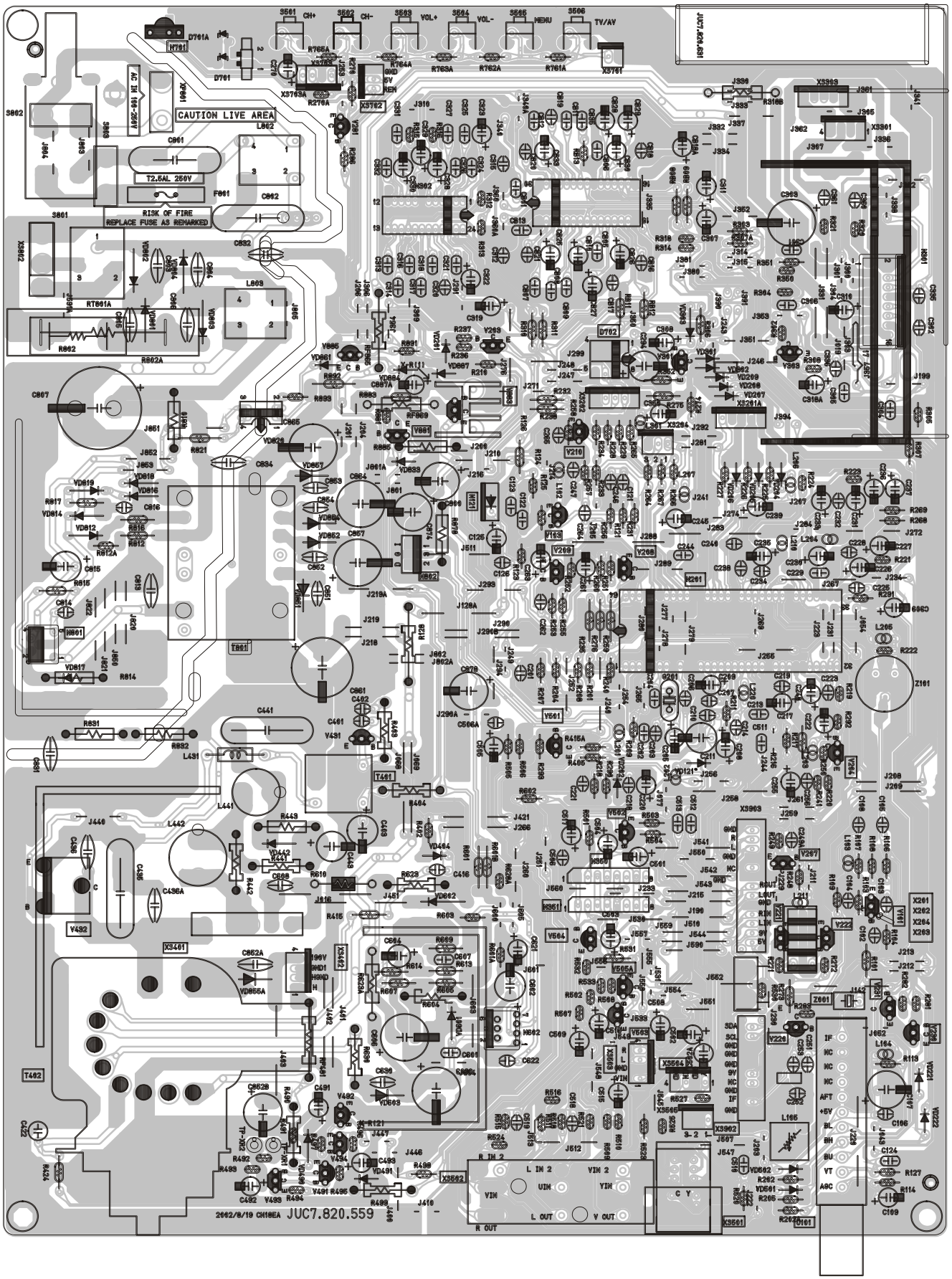


Serial No.	Code No.	Parts	Qty	Remarks
33				
32		White nitro magnetic paint Q04-3		
31		Soldering agent		
30		Tin solder		
29		Plasticine		
28			1	
27		Protection film 2124 - width=250mm	1.2m	
26		Binding wire XJ-100	1	
UL 25		Notched nut M5K	4	Only for Sag Hitachi GS CRTs
24			4	
23			4	
22	Japan Standard	Tapping screw 4 20BABh	6	
21	Japan Standard	Tapping screw 4 16BTBh	4	
20	Japan Standard	Tapping screw 3 12VwWCh	4	
19		Notched nut M5	4	Not for Sag Hitachi CRT
18	T/JU8.949.224	Washer	4	
17		Model No. label	1	
16			1	
15			1	
14	JUC8.667.011	Wire clip A	1	Black
UL 13	T/JU8.667.328	Wire clip A	1	
12	T/JU8.667.310	Wire clip	2	
11	T/JU8.676.003	Distance clip	1	
10			1	
9		AV plate	1	
UL 8	JUC8.077.213	Rear terminals	1	HQ - 1
7	JUC8.074.320	Back cover	1	HQ - 1
6		Main PCB assembly	1	
5		CRT RGB PCB assembly	1	
4			1	
3	JUC6.116.639	Front cover assembly	1	
2		CRT assembly	1	
1			1	

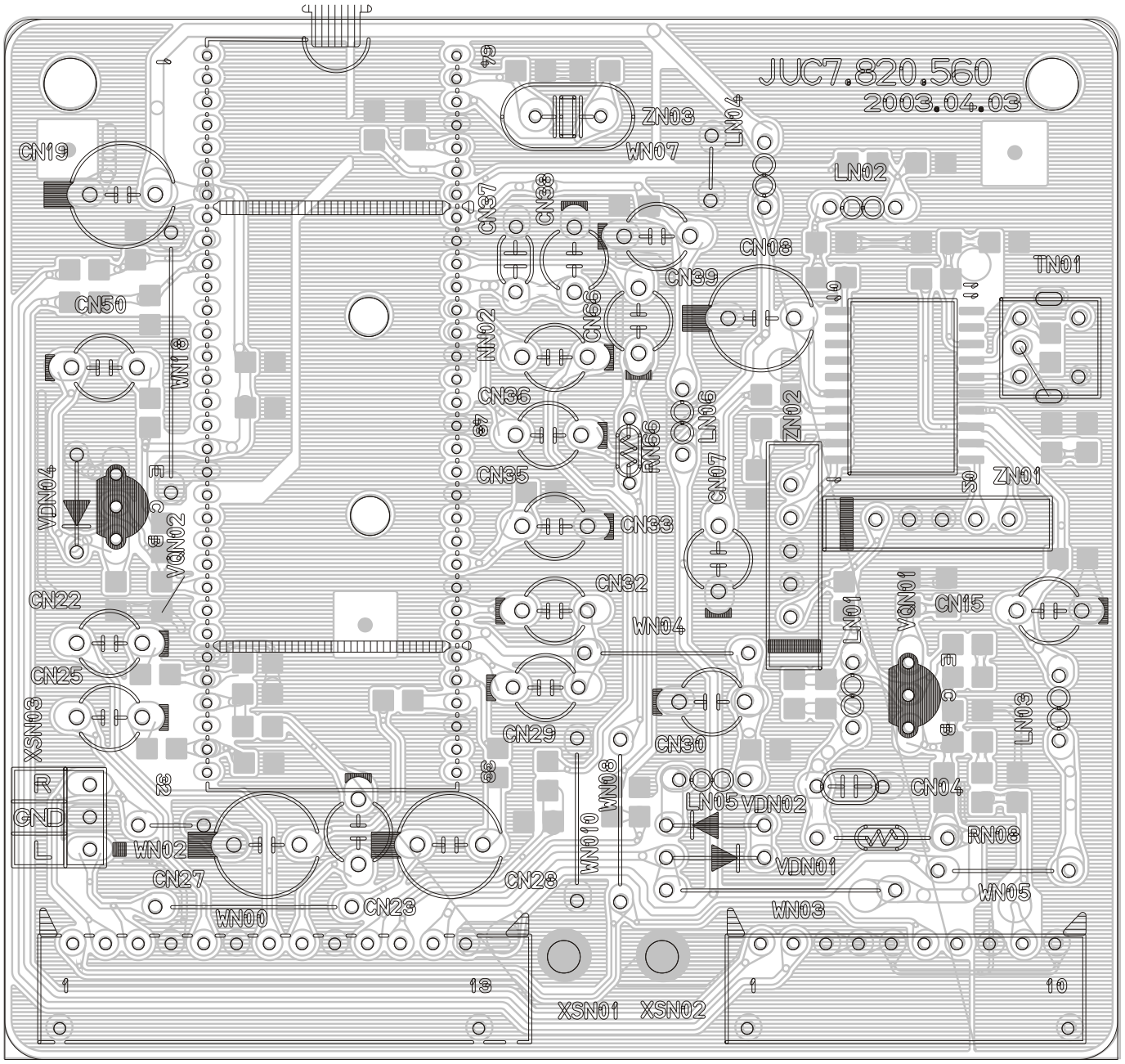
FINAL WIRING DIAGRAM FOR 21E88



PRINTED CIRCUIT BOARD DIAGRAM (1)



PRINTED CIRCUIT BOARD DIAGRAMS (2)



PRINTED CIRCUIT BOARD DIAGRAMS（3）